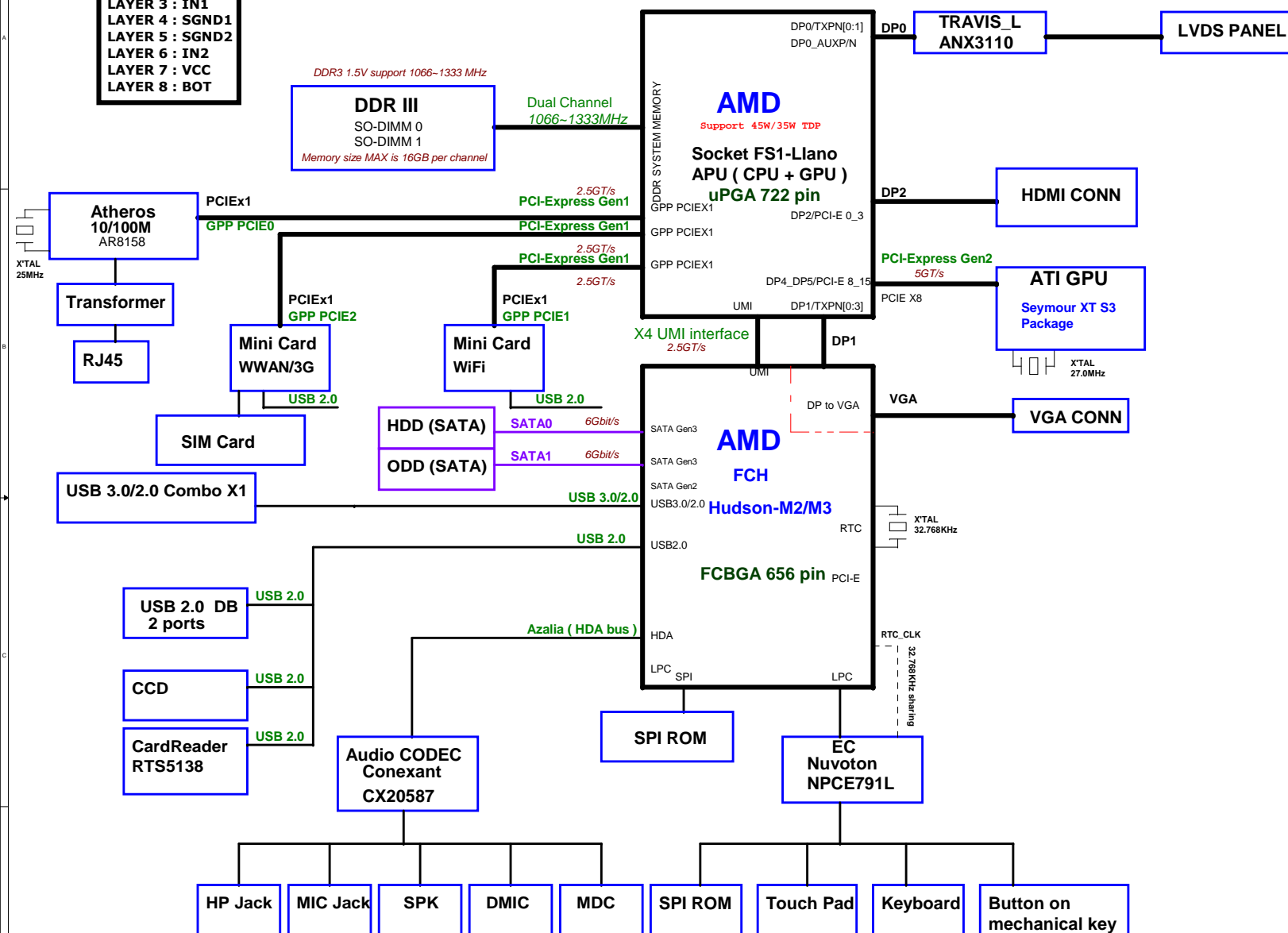


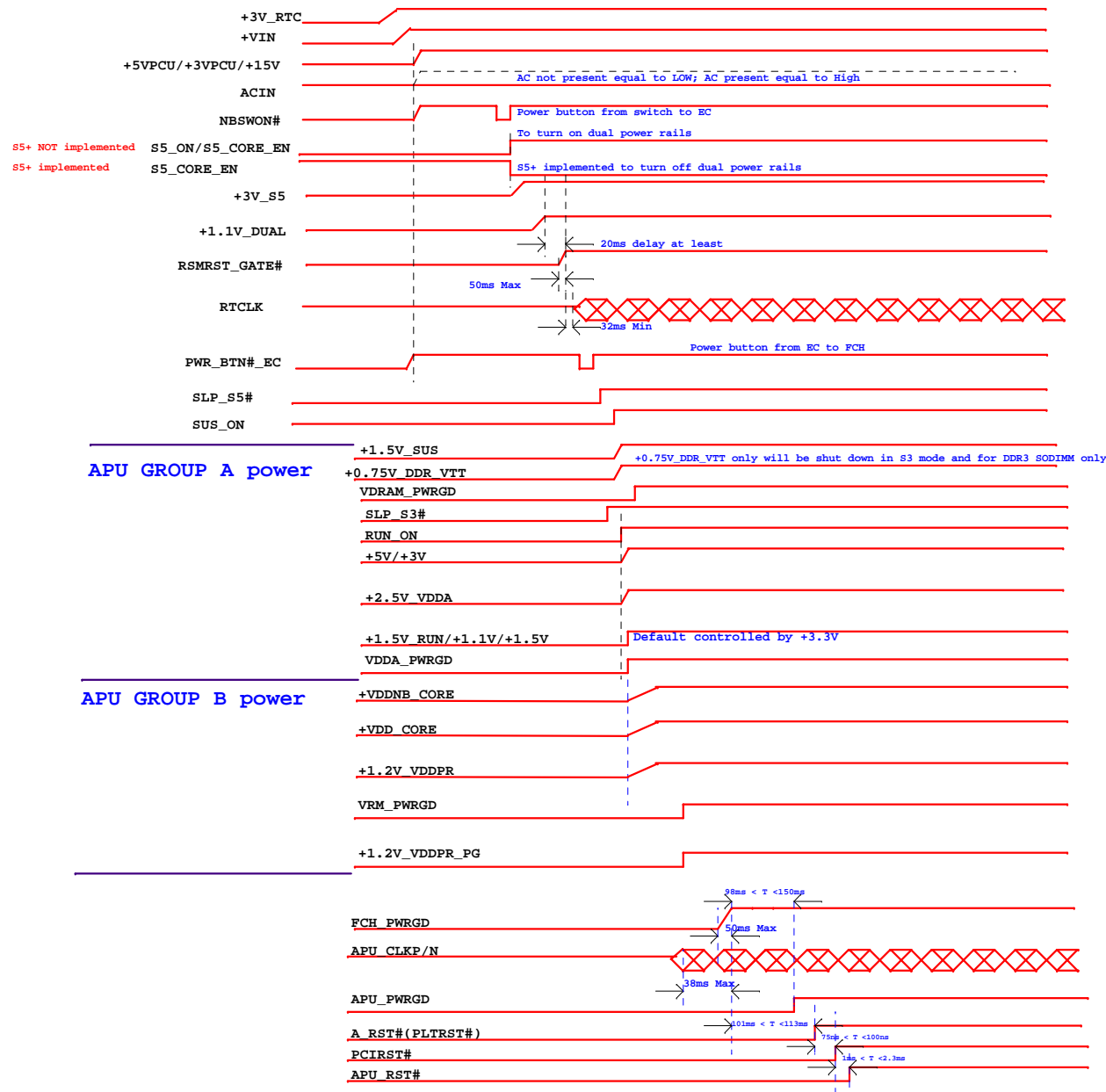
PCB STACK UP

LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : SGND1
 LAYER 5 : SGND2
 LAYER 6 : IN2
 LAYER 7 : VCC
 LAYER 8 : BOT

BLOCK DIAGRAM



BLF/BLFD Power On Sequence: S5 > S0



APU Power on sequence required:

Llano APU:

- 1.Group A (+1.5V_SUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M2/M3:

- 1.+3V_S5 ramp before +1.1V_DUAL
- 2.+3V ramp before +1.1V
- 3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Seymour XT S3 package Power-on sequence

All power rails reach nominal within 20ms

- 1=> +3V_GPU
- 2=> +VGPU_CORE/+1V_GPU
- 3=> +VGPU_CORE PWRGD to enable +1.5V_GPU
- 4=> +1V_GPU PWRGD to enable +1.8V_GPU

NOTE

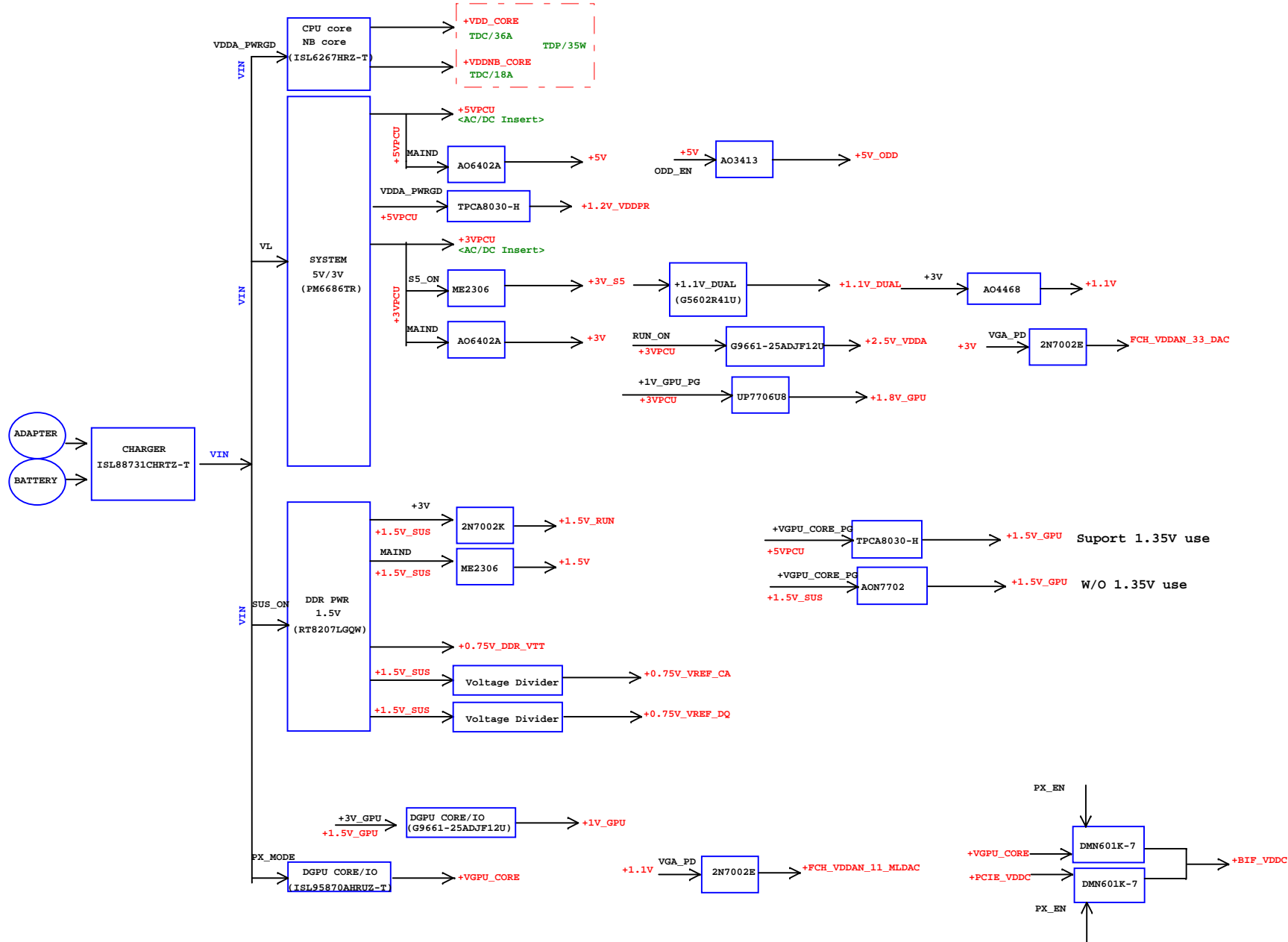
- 1.+3V to turn on +3V_GPU
- 2.+3V_GPU ready to enable +VGPU_CORE/+1V_GPU (+1V_GPU will ramp up before +VGPU_CORE)
- 3.+VGPU_CORE PWRGD to enable +1.5V_GPU
- 3.+1V_GPU PWRGD to enable +1.8V_GPU

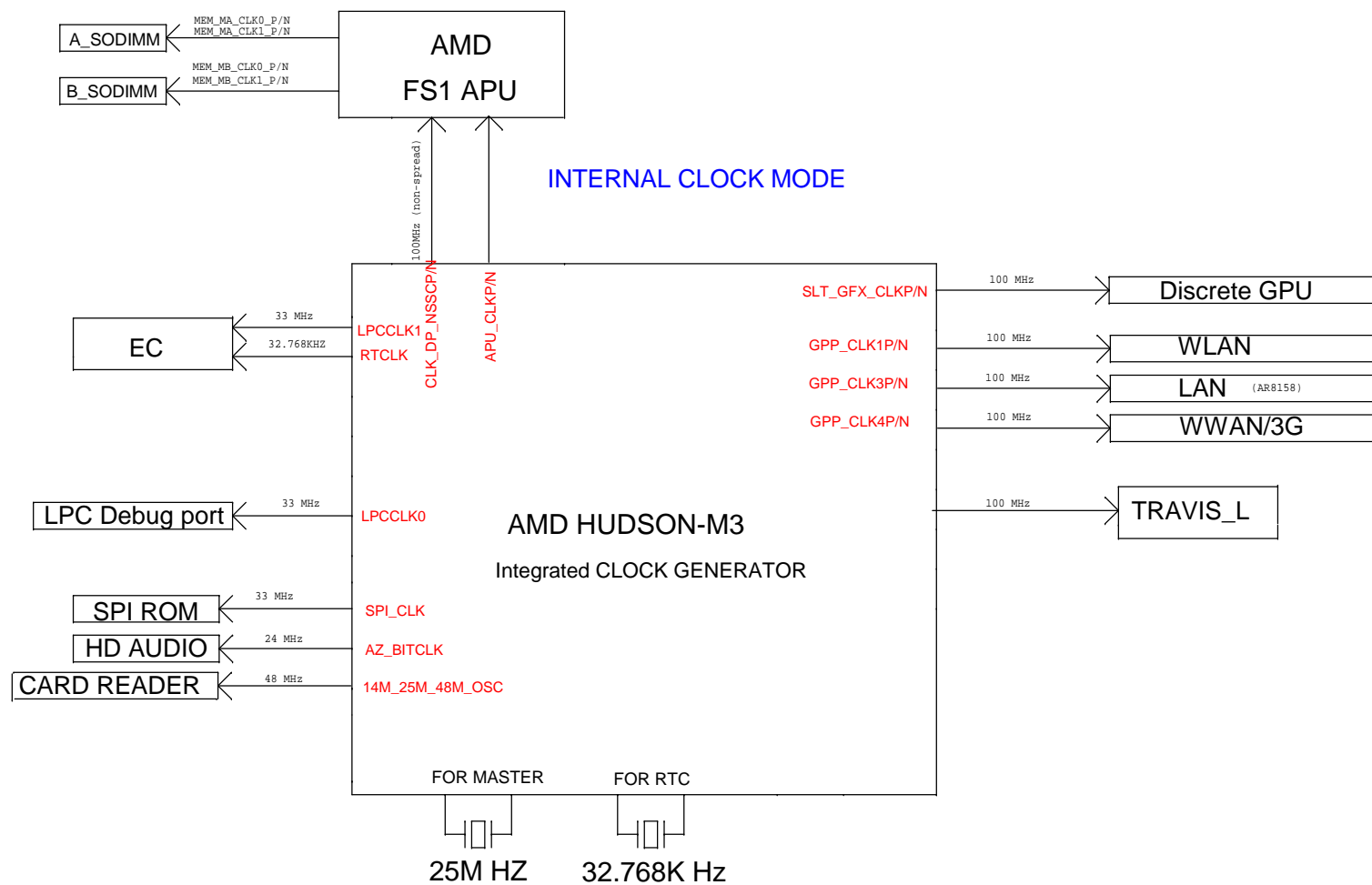
TRAVIS_L ANX3110 power on sequence

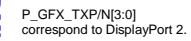
- 1.+3V must lead +1.2V_TRAVIS

- 2.+1.2V_TRAVIS must lead TRAVIS_RST#


NOTE: FCH must output PCIE_RST#_TRAVIS or APU_PCIE_RST# after +1.2V_TRAVIS ready

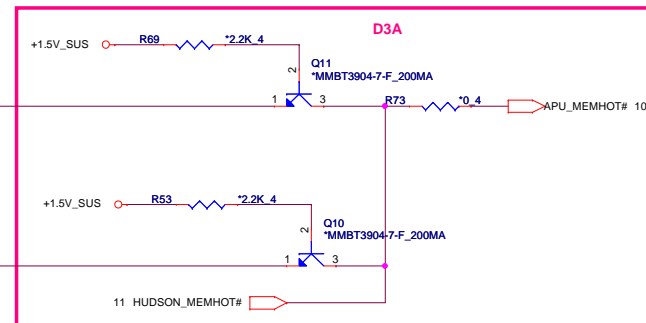
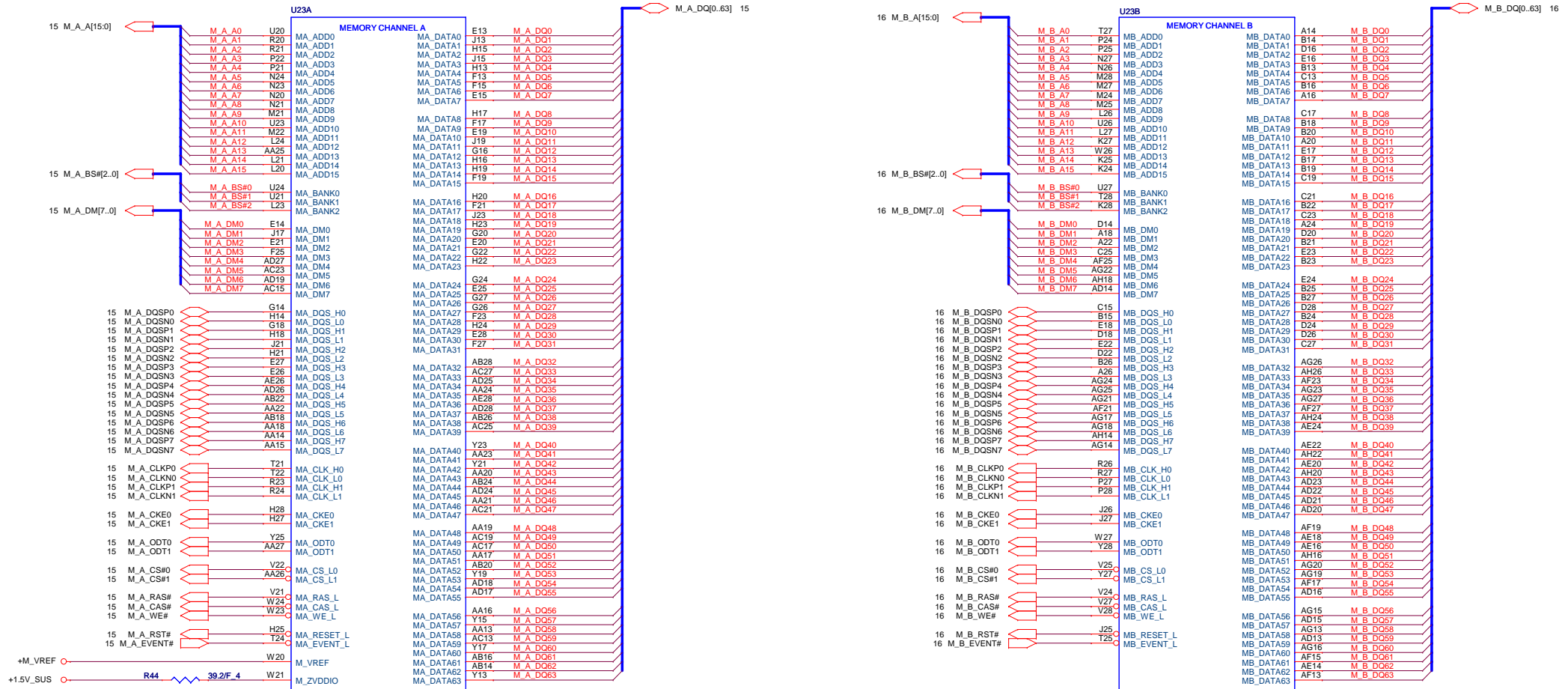






LAN
WLAN
3G

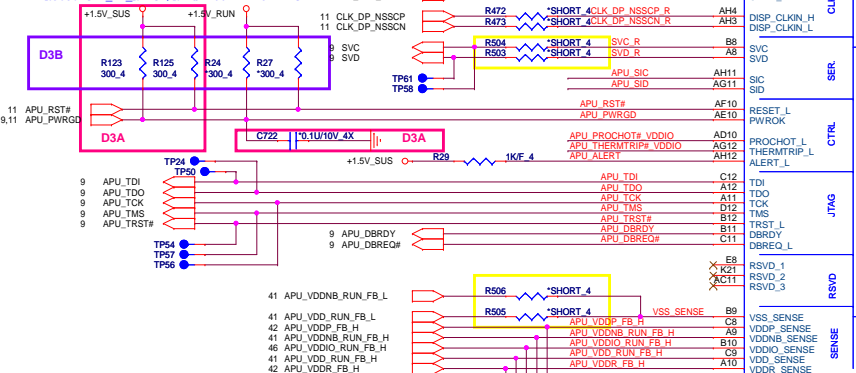
 <div> Quanta Computer Inc. PROJECT : BLF_BLFD </div>			
Size	Document Number	Rev	
	Llano PCIE/UMI/GPP	1C	
Date:	Tuesday, April 19, 2011	Sheet	5 of 53



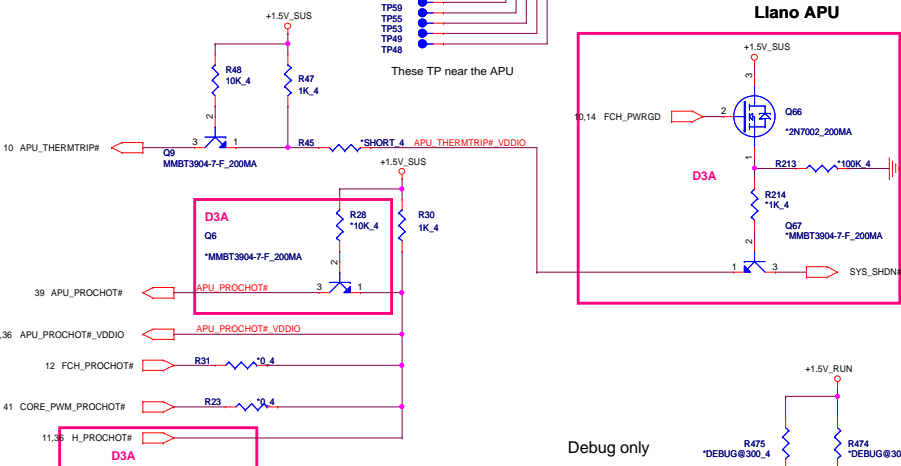
DP0 to LVDS

DP1 to Hudson-M3 VGA output

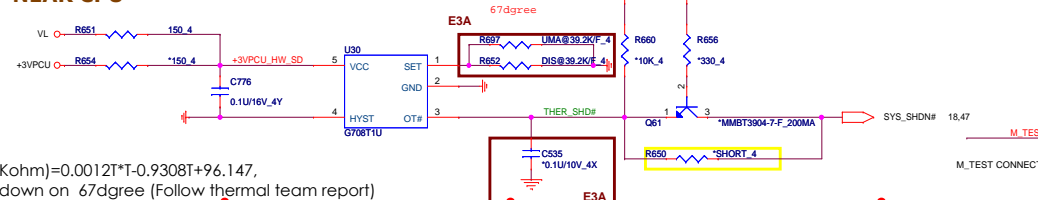
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC



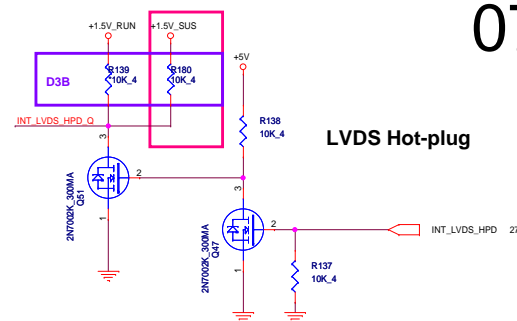
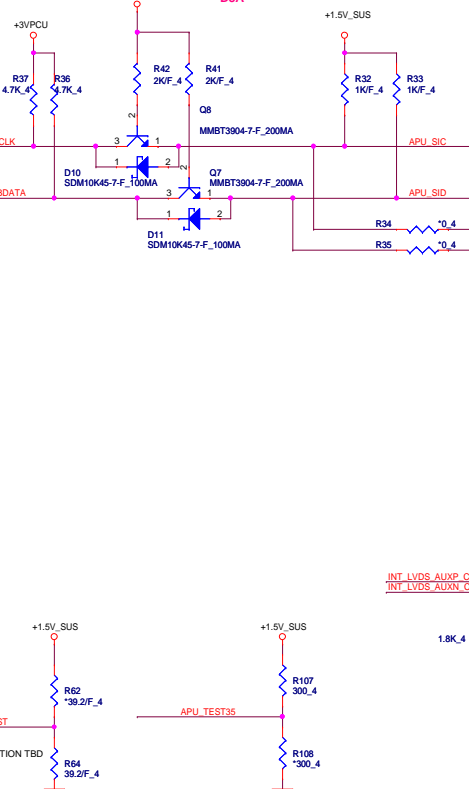
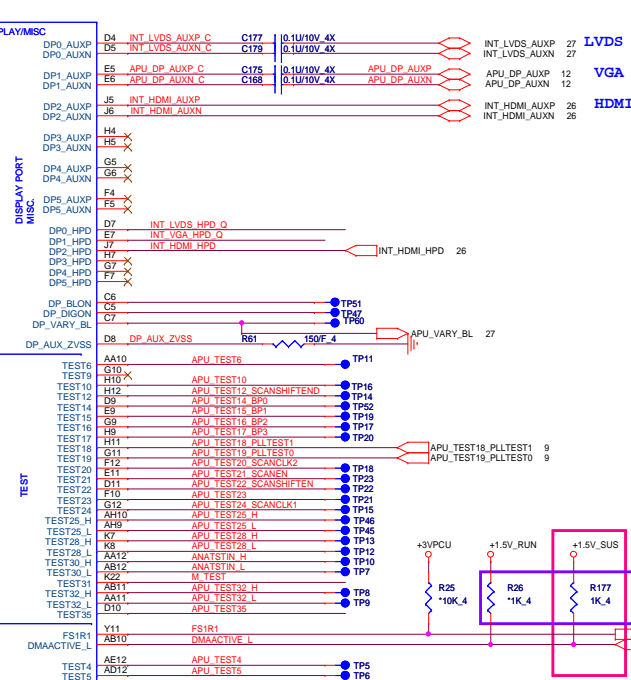
Llano APU



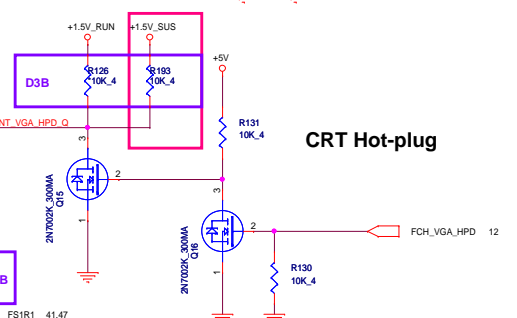
NEAR CPU



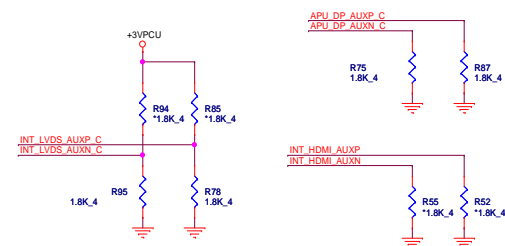
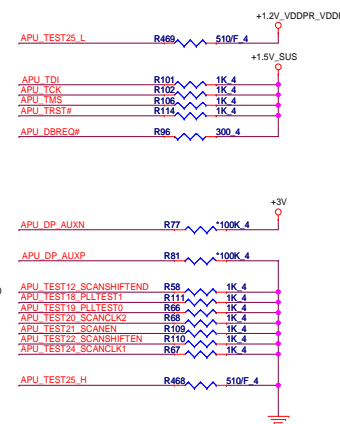
Rset(Kohm)=0.0012T-0.9308T+96.147,
Shut down on 67dgree (Follow thermal team report)
Hysteresis is 30C



LVDS Hot-plug

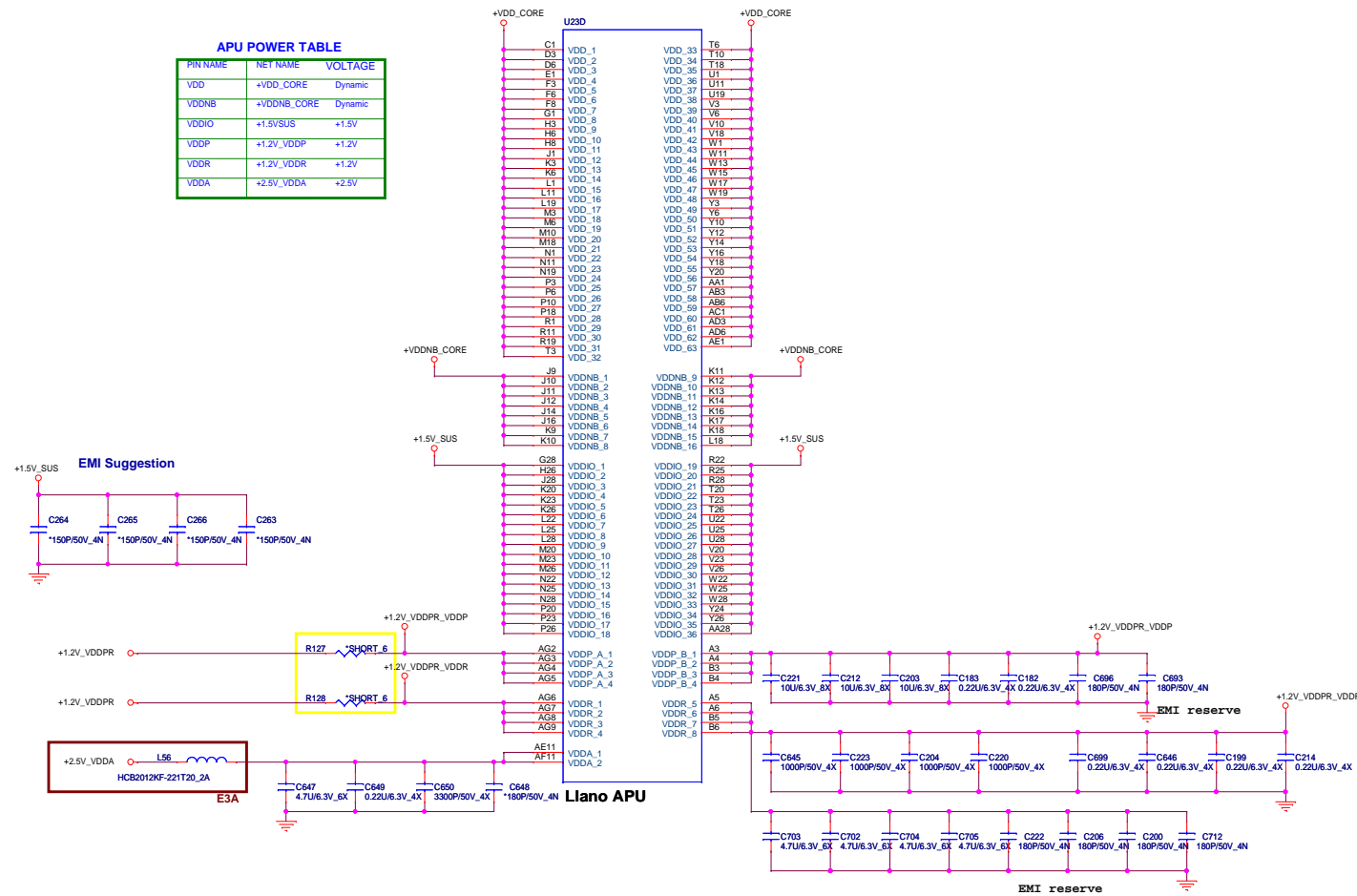


CRT Hot-plug



APU POWER TABLE

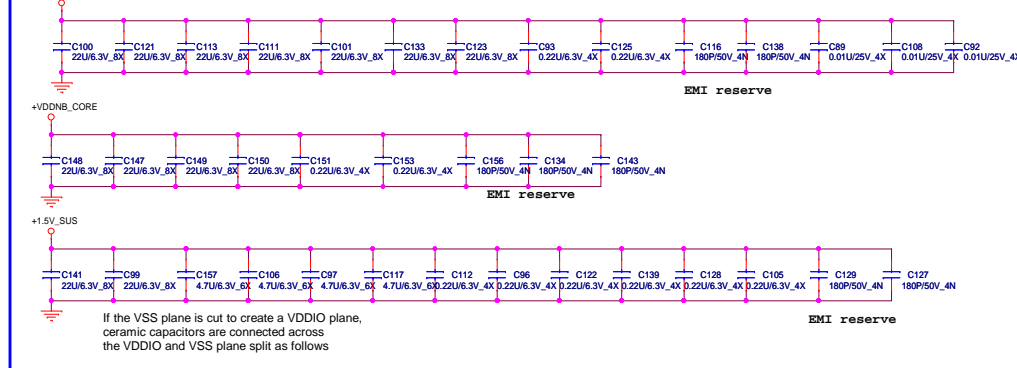
PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	Dynamic
VDDNB	+VDDNB_CORE	Dynamic
VDDIO	+1.5V_SUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



U23E		
A7	VSS_1	T11
A13	VSS_2	T19
A15	VSS_3	T4
A17	VSS_4	T7
A19	VSS_5	T10
A21	VSS_6	T18
A23	VSS_7	T11
A25	VSS_8	T19
B7	VSS_9	T4
B9	VSS_10	T7
C10	VSS_11	T10
C14	VSS_12	T18
C16	VSS_13	T11
C18	VSS_14	T19
C20	VSS_15	T4
C22	VSS_16	T7
C24	VSS_17	T10
C26	VSS_18	T18
C28	VSS_19	T11
D13	VSS_20	T19
D15	VSS_21	T4
D17	VSS_22	T7
D19	VSS_23	T10
D21	VSS_24	T18
D23	VSS_25	T11
D25	VSS_26	T19
D27	VSS_27	T4
E4	VSS_28	T7
E10	VSS_29	T10
E12	VSS_30	T18
F9	VSS_31	T11
F11	VSS_32	T19
F14	VSS_33	T4
F16	VSS_34	T7
F18	VSS_35	T10
F20	VSS_36	T18
F22	VSS_37	T11
F24	VSS_38	T19
F26	VSS_39	T4
F28	VSS_40	T7
G4	VSS_41	T10
G8	VSS_42	T18
G13	VSS_43	T11
G15	VSS_44	T19
G17	VSS_45	T4
G19	VSS_46	T7
G21	VSS_47	T10
G23	VSS_48	T18
G25	VSS_49	T11
J4	VSS_50	T19
J8	VSS_51	T4
J18	VSS_52	T7
J20	VSS_53	T10
J22	VSS_54	T18
J24	VSS_55	T11
K19	VSS_56	T19
L10	VSS_57	T4
L7	VSS_58	T7
M11	VSS_59	T10
M19	VSS_60	T18
N4	VSS_61	T11
N7	VSS_62	T19
N10	VSS_63	T4
N18	VSS_64	T7
P9	VSS_65	T10
P11	VSS_66	T18
P19	VSS_67	T11
R4	VSS_68	T19
R7	VSS_69	T4
R10	VSS_70	T7
R18	VSS_71	T10
T9	VSS_72	T18
	VSS_73	T11
	VSS_74	T19

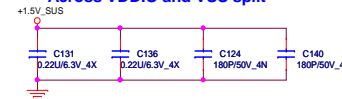
Liano APU

BOTTOM SIDE DECOUPLING

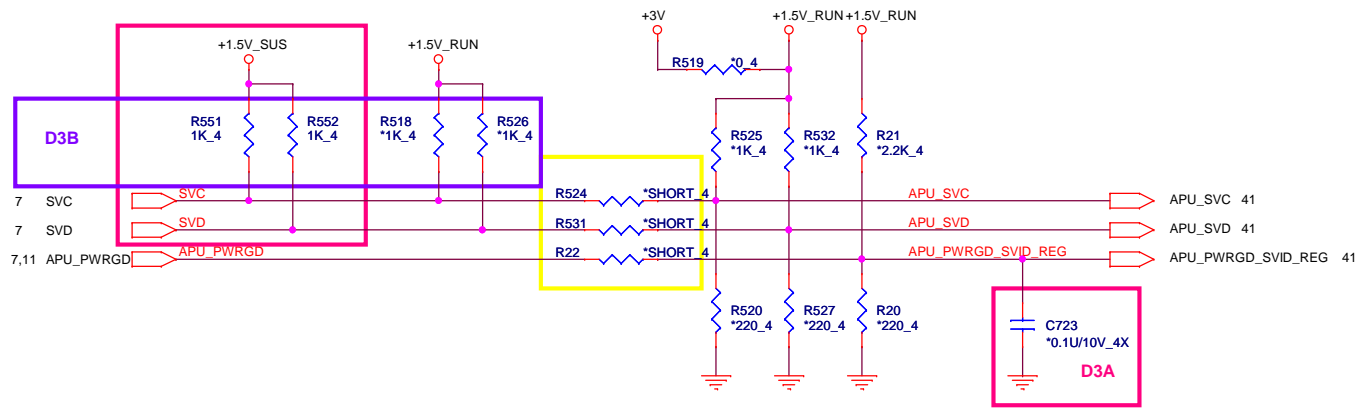


DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split

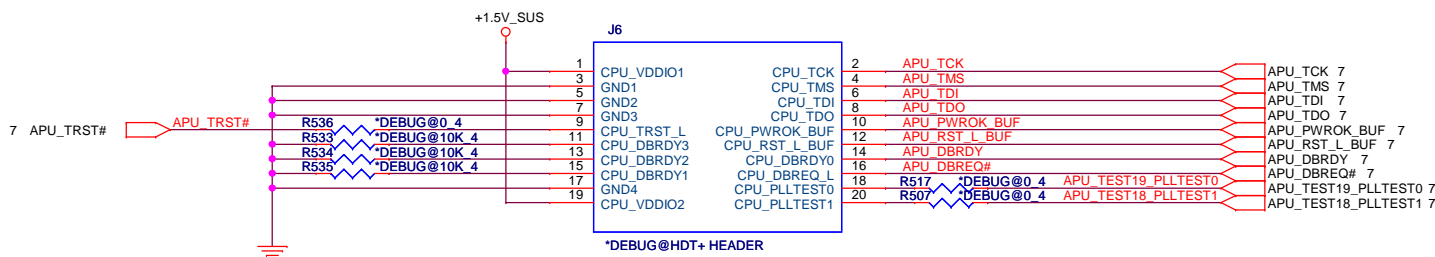



VID Override Circuit



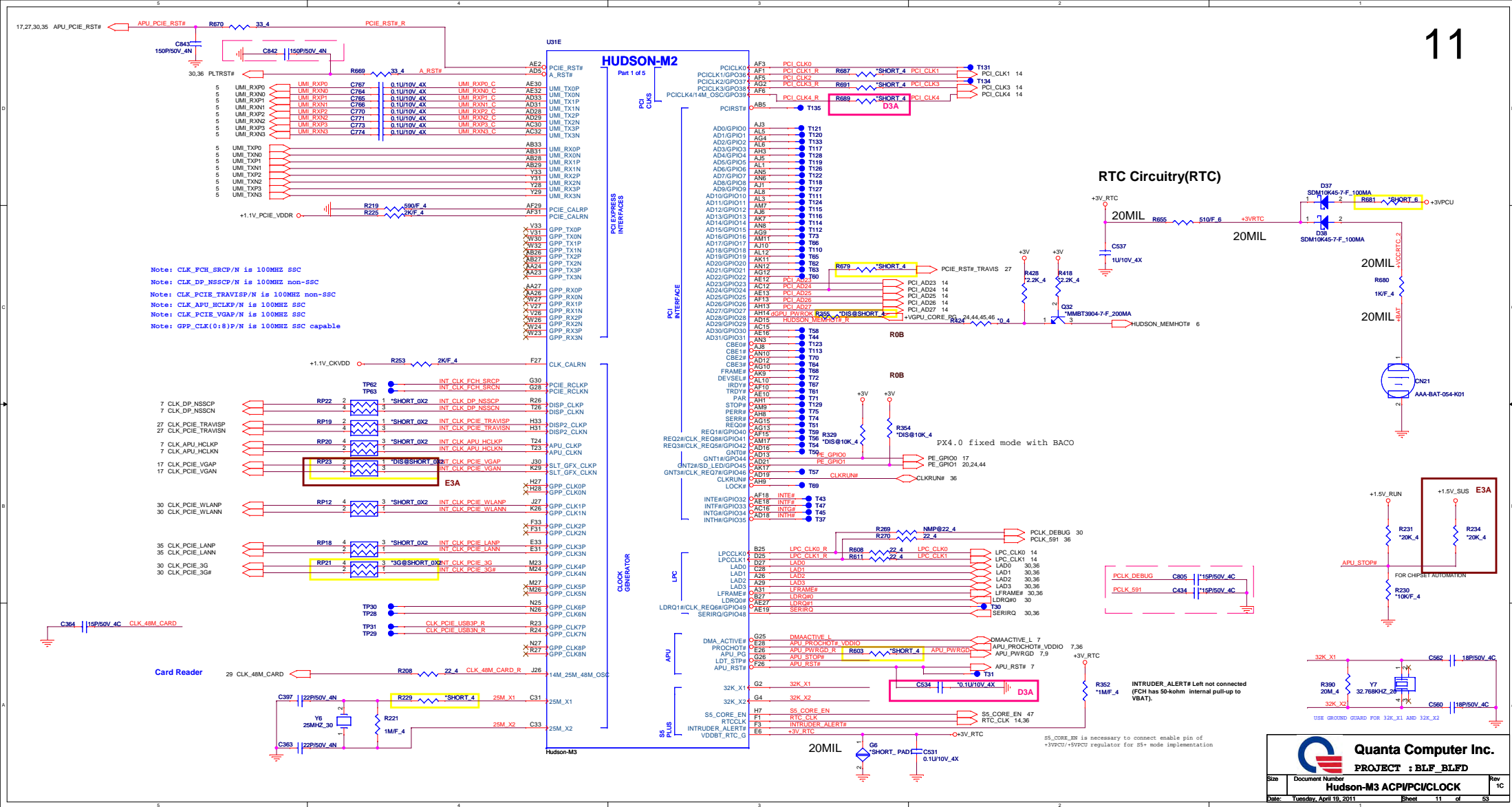
HDT+ Connector

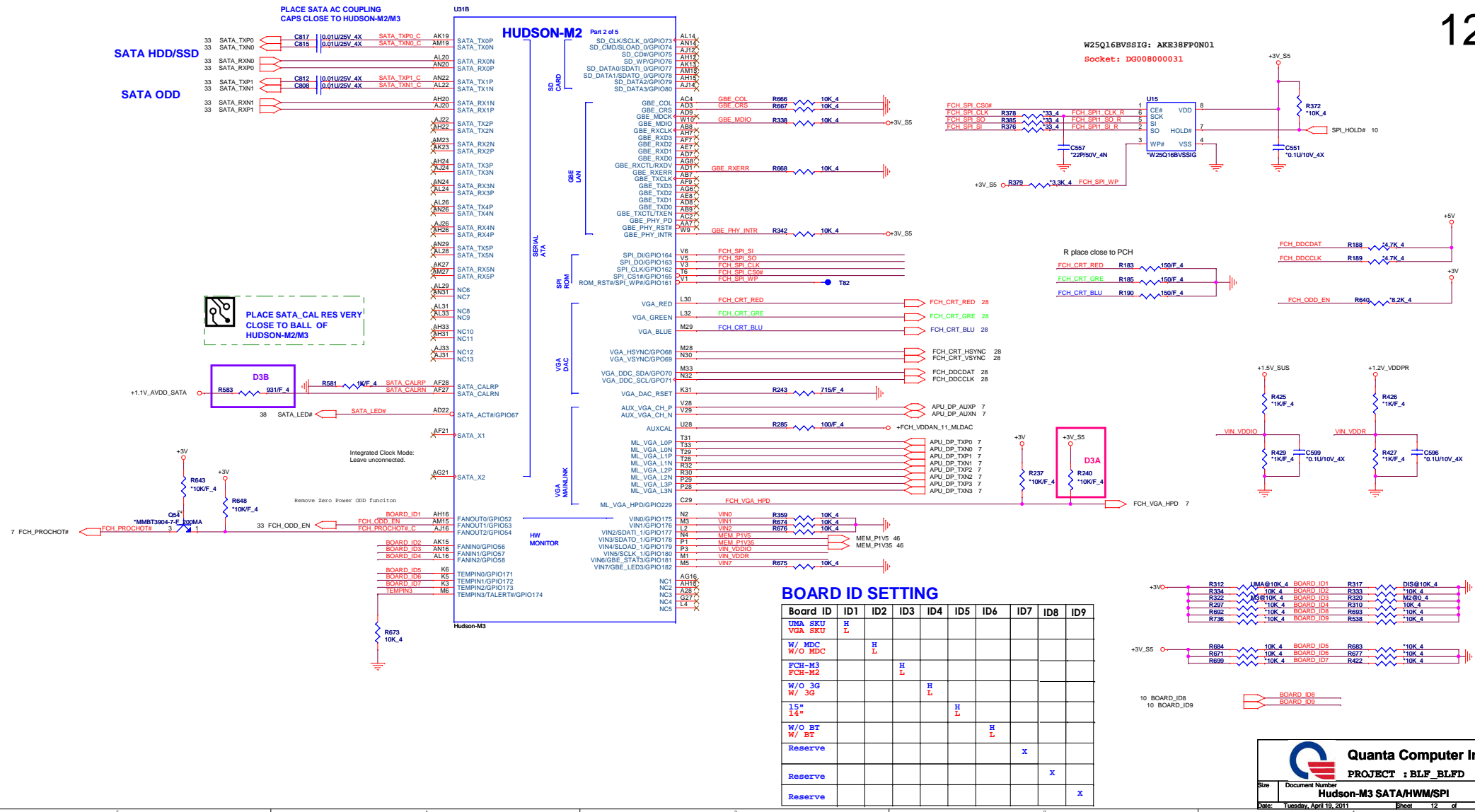
Debug only



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Llano DEBUG&OTHER		
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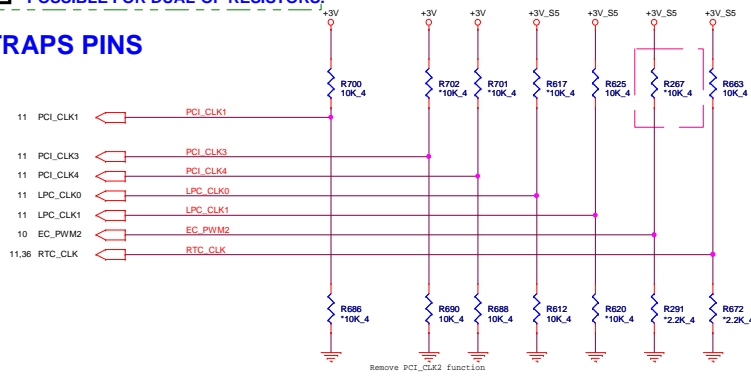


VDD-- S/B CORE power



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS



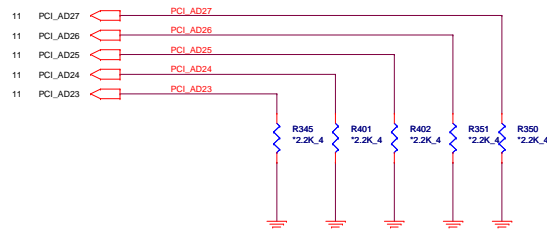
EC_PWM2-->
SPI ROM: 2.2-KΩ 5k pull-down
LPC ROM: Pull-up to 3.3V_S5.
External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

REQUIRED STRAPS

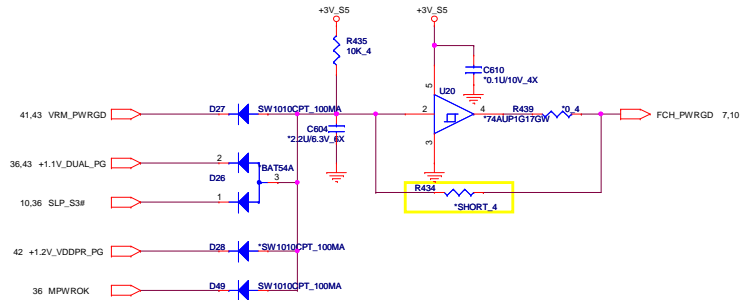
		PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH		ALLOW PCIe Gen2 DEFAULT		USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW		FORCE PCIe Gen1		IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



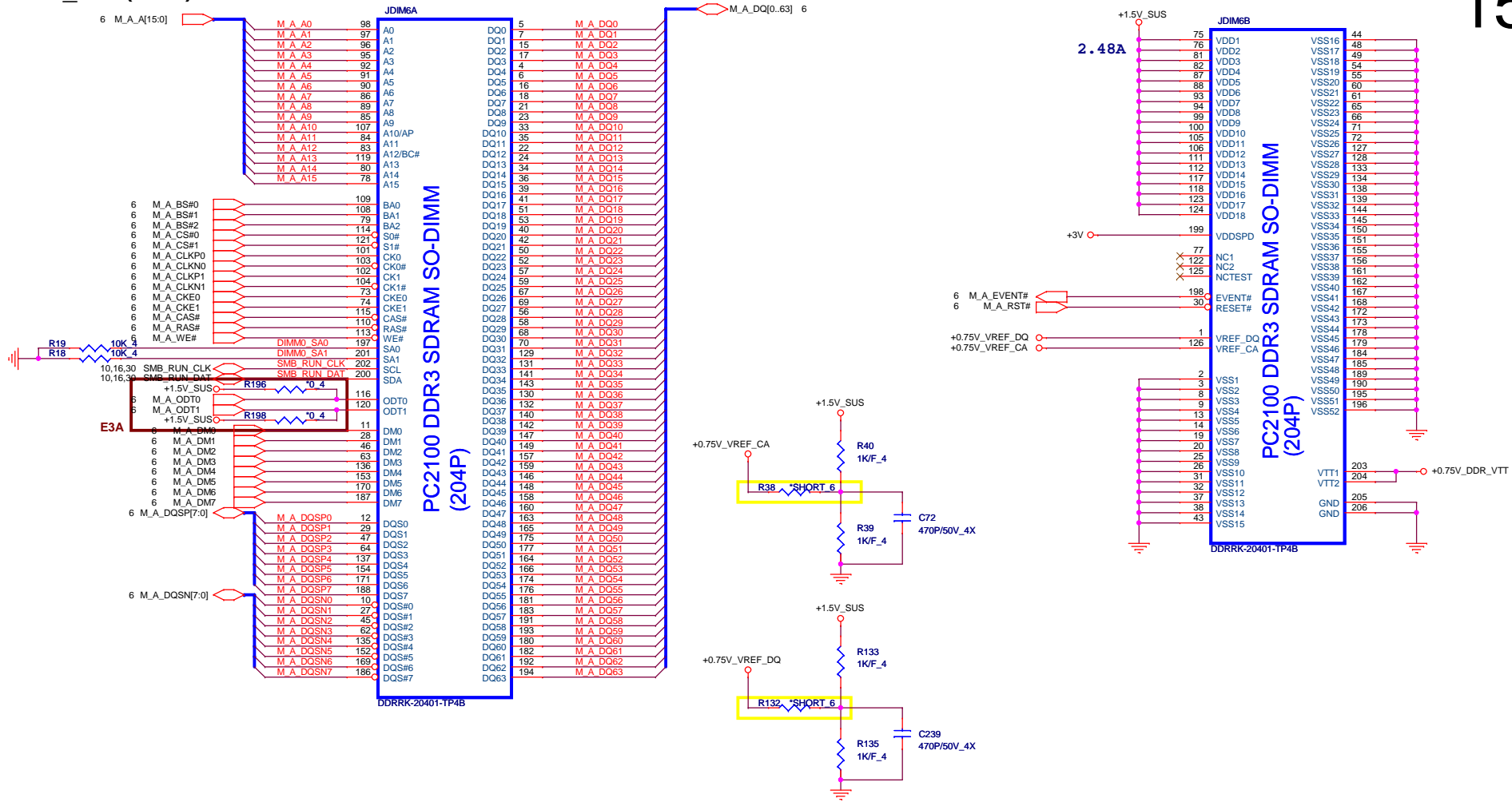
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT



FCH PWRGD CKT

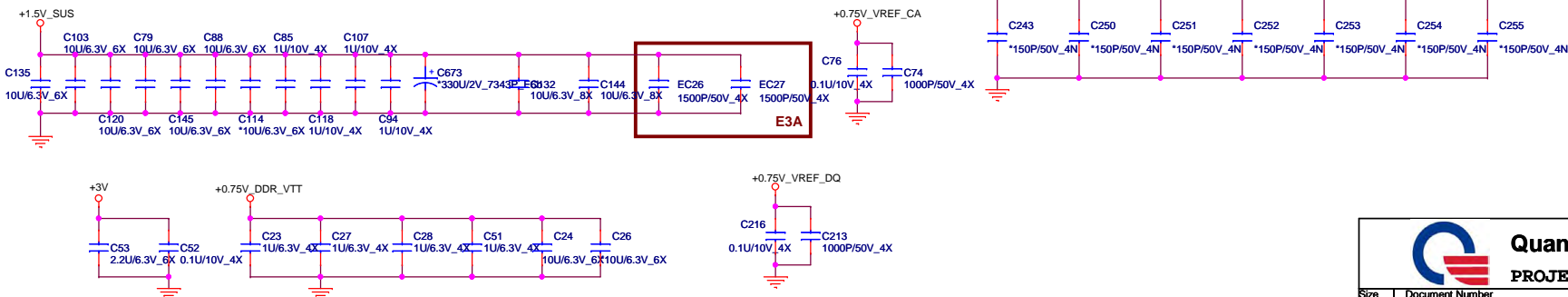
DDR_STD (DDR)

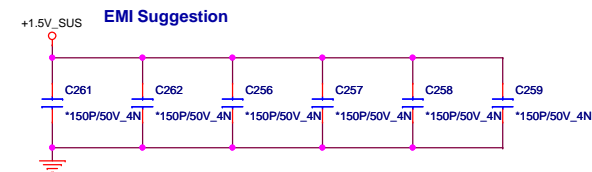
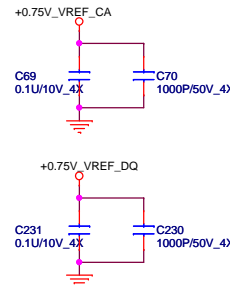
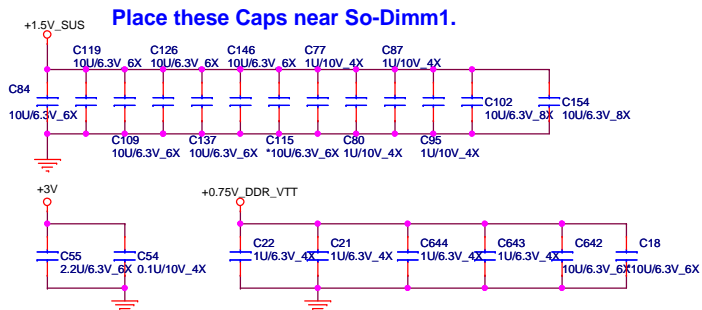
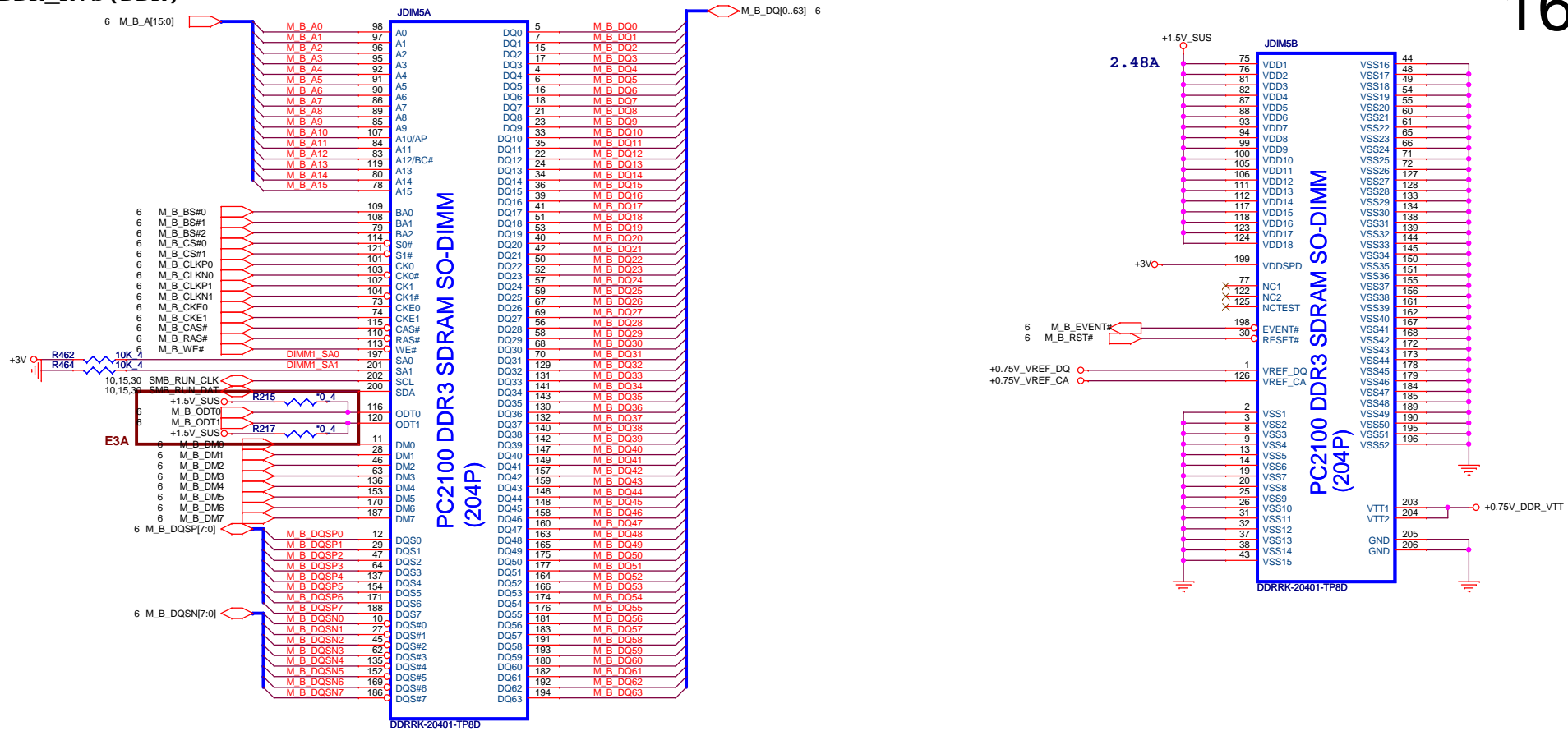
15

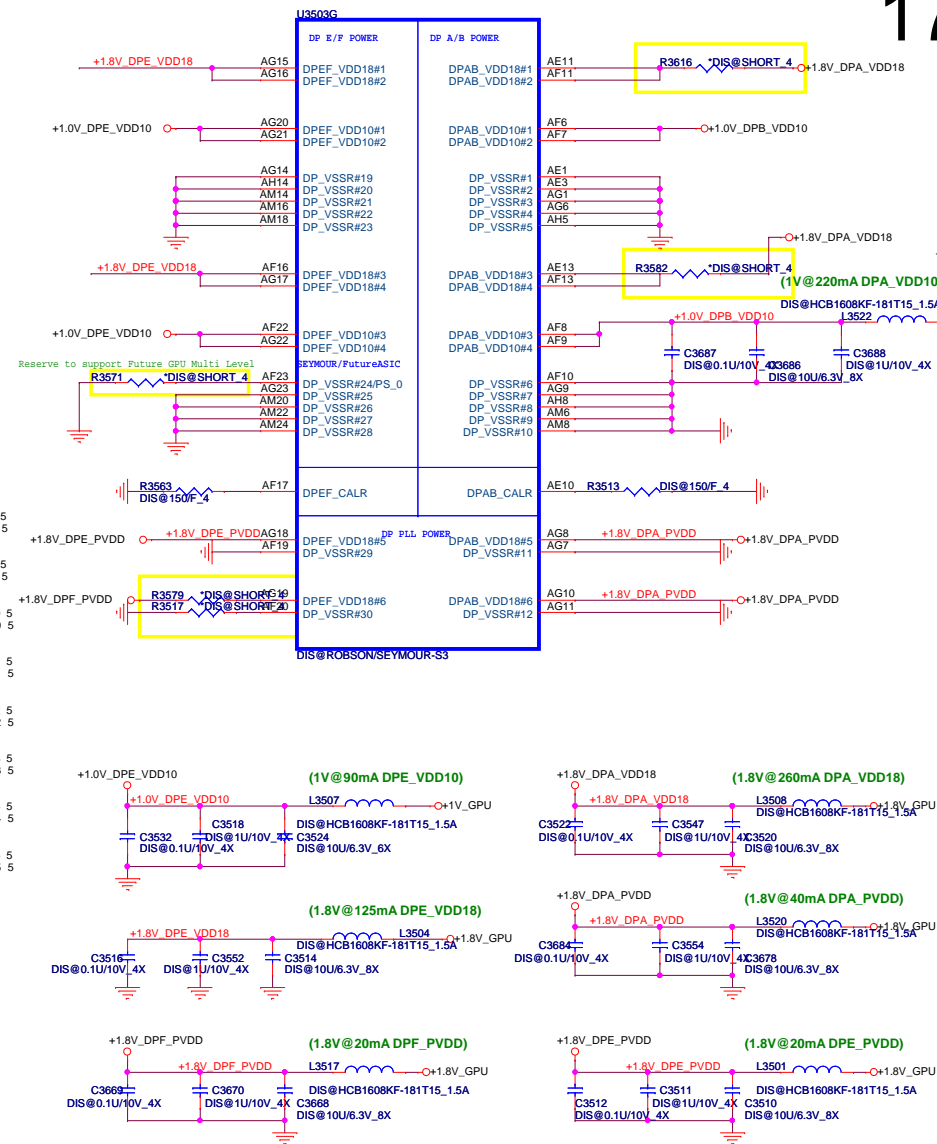
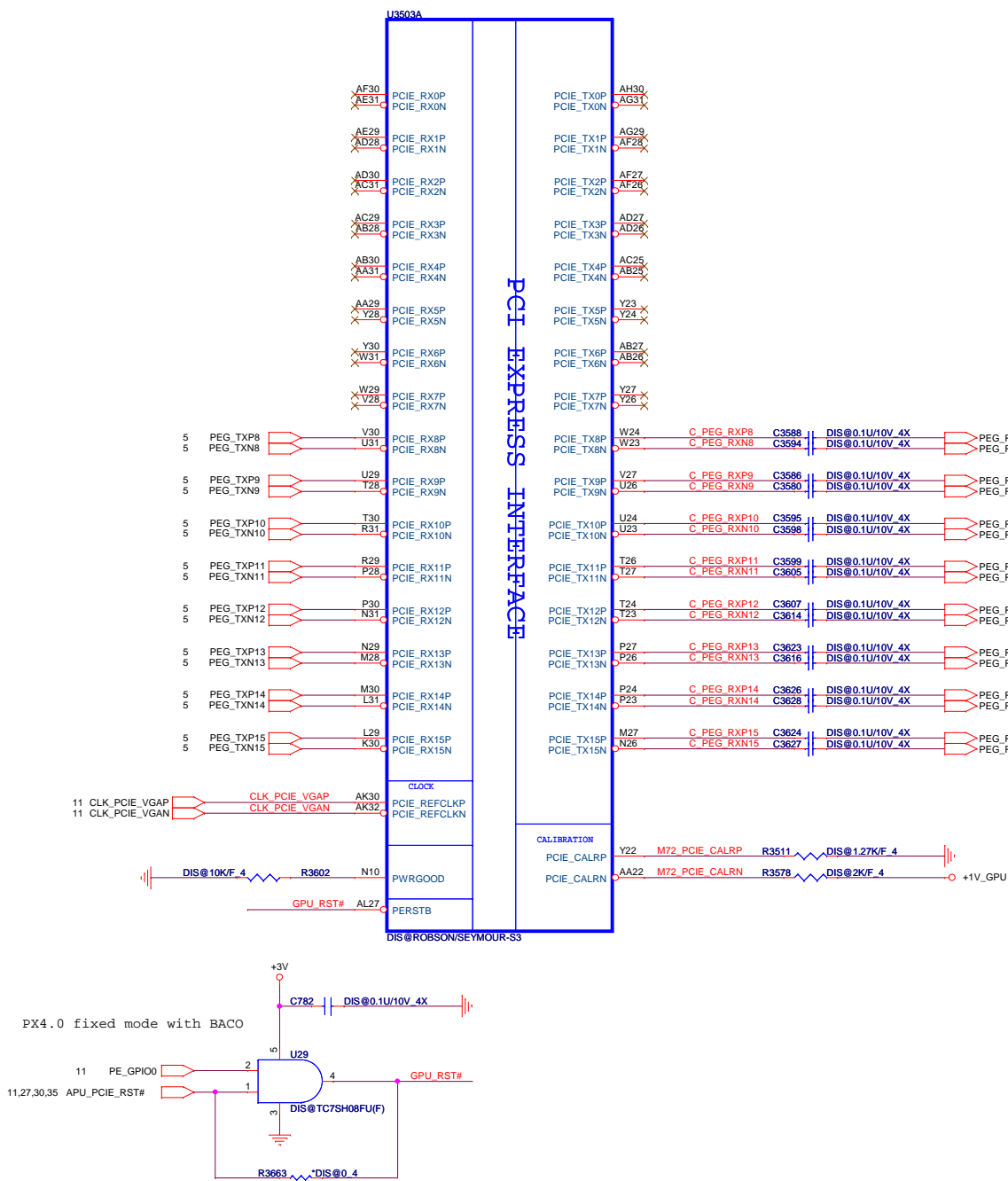


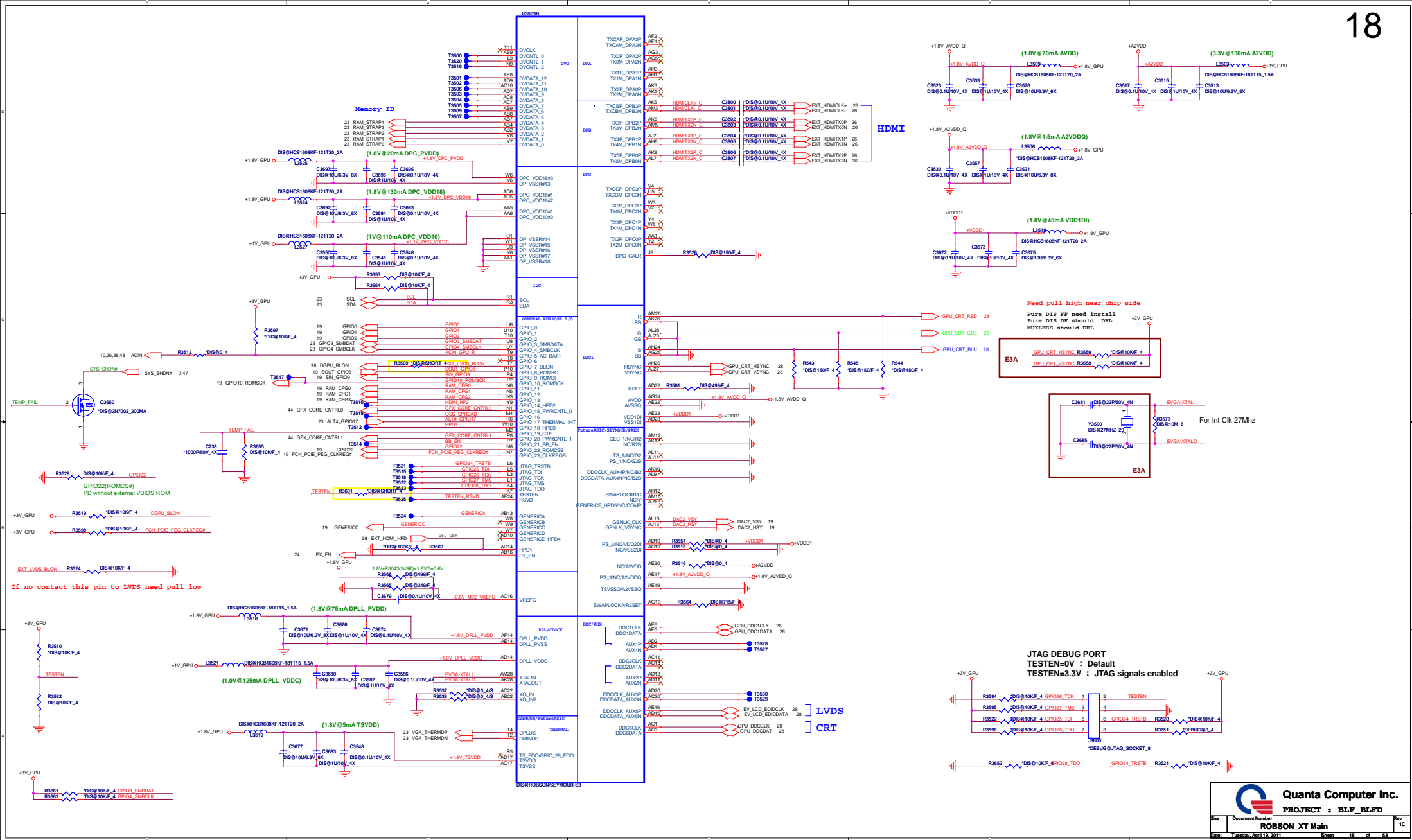
Place these Caps near SoDimm0.

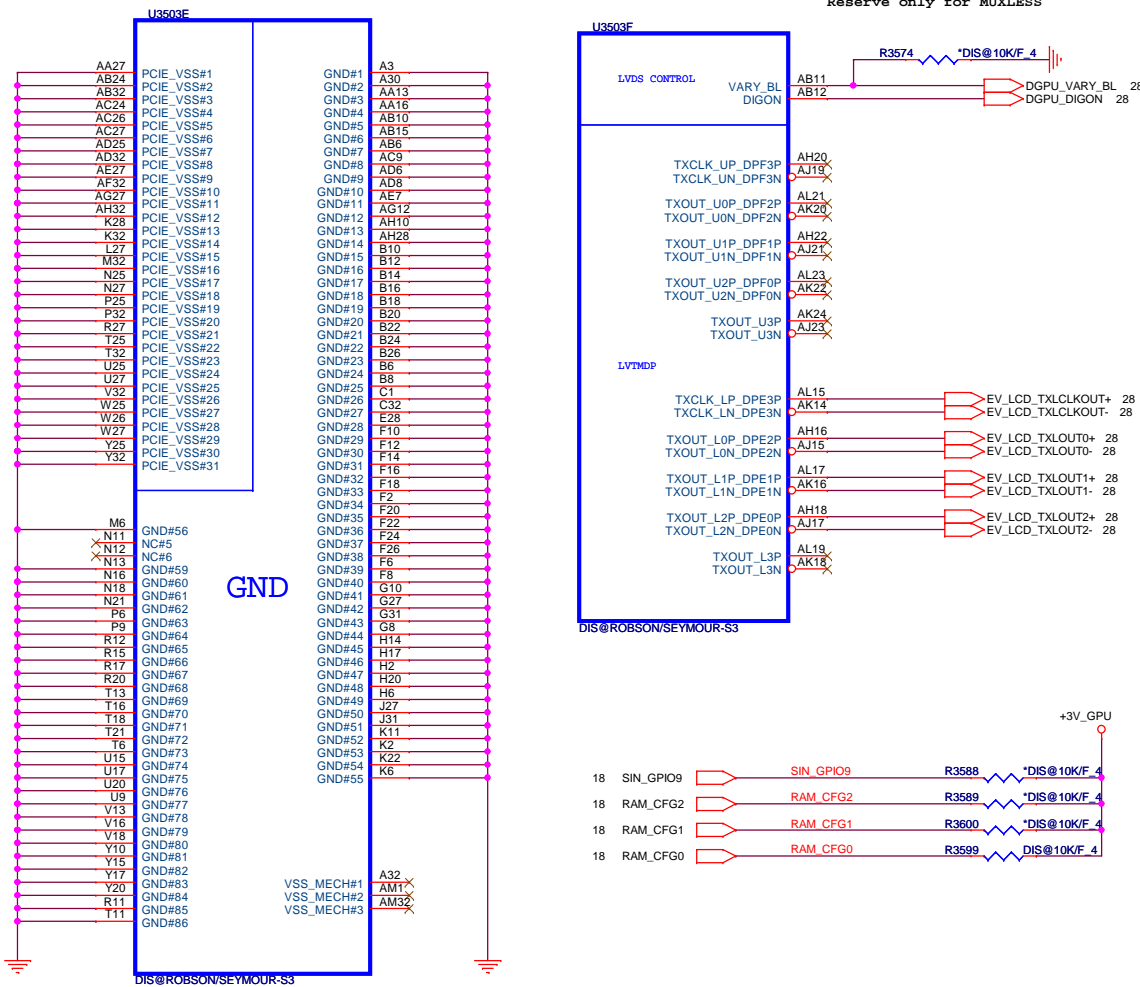
EMI Suggestion











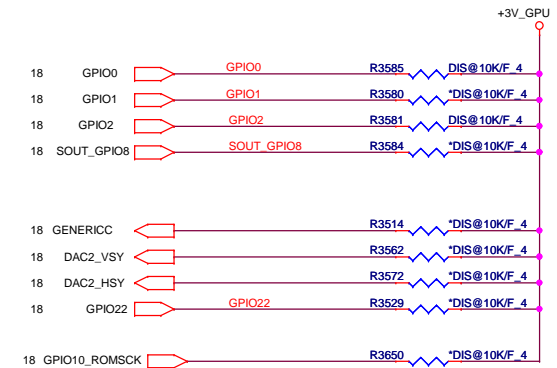
CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

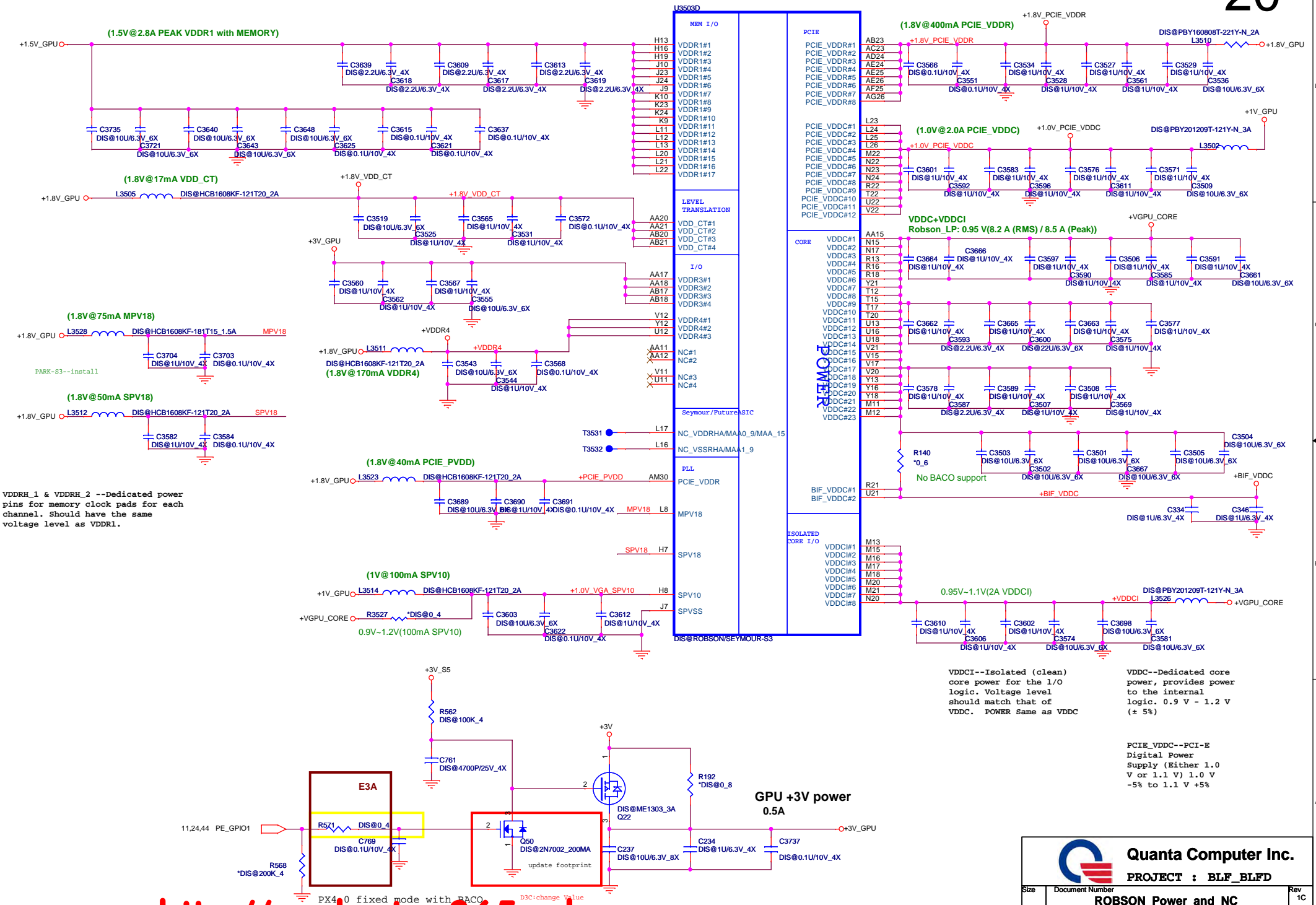
AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

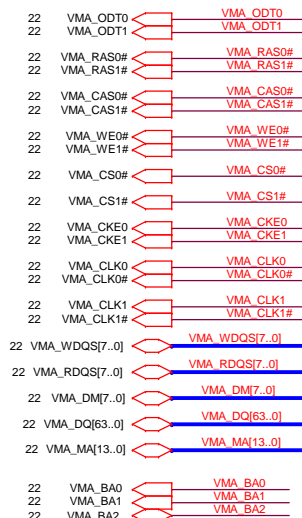
Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

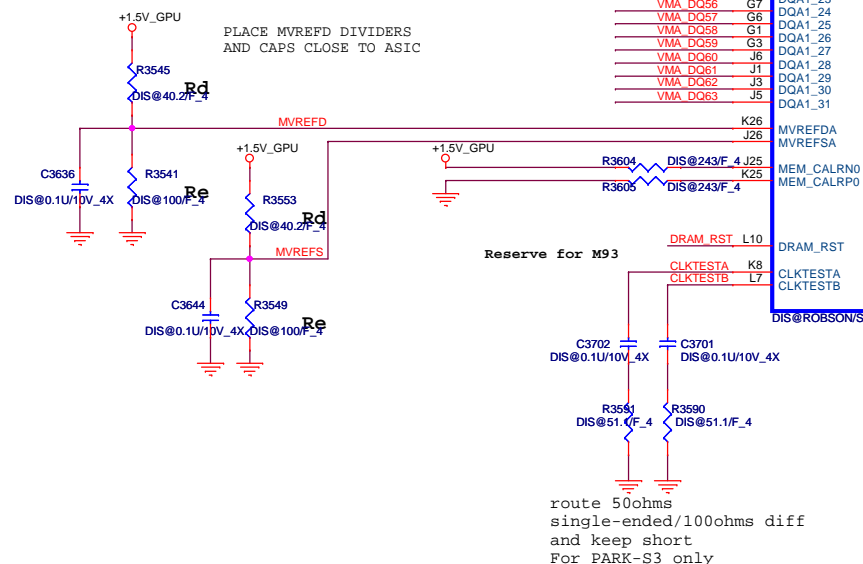






support 1gbt
VRAM (64M X 16)

DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

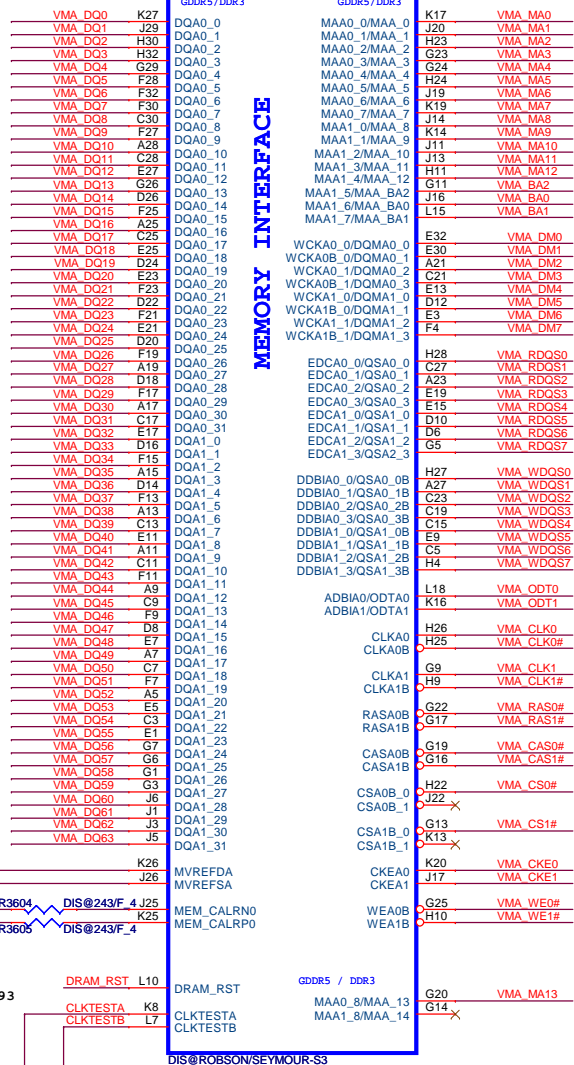


route 50ohms
single-ended/100ohms diff
and keep short
For PARK-S3 only

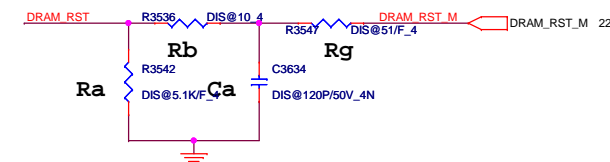
U3503C

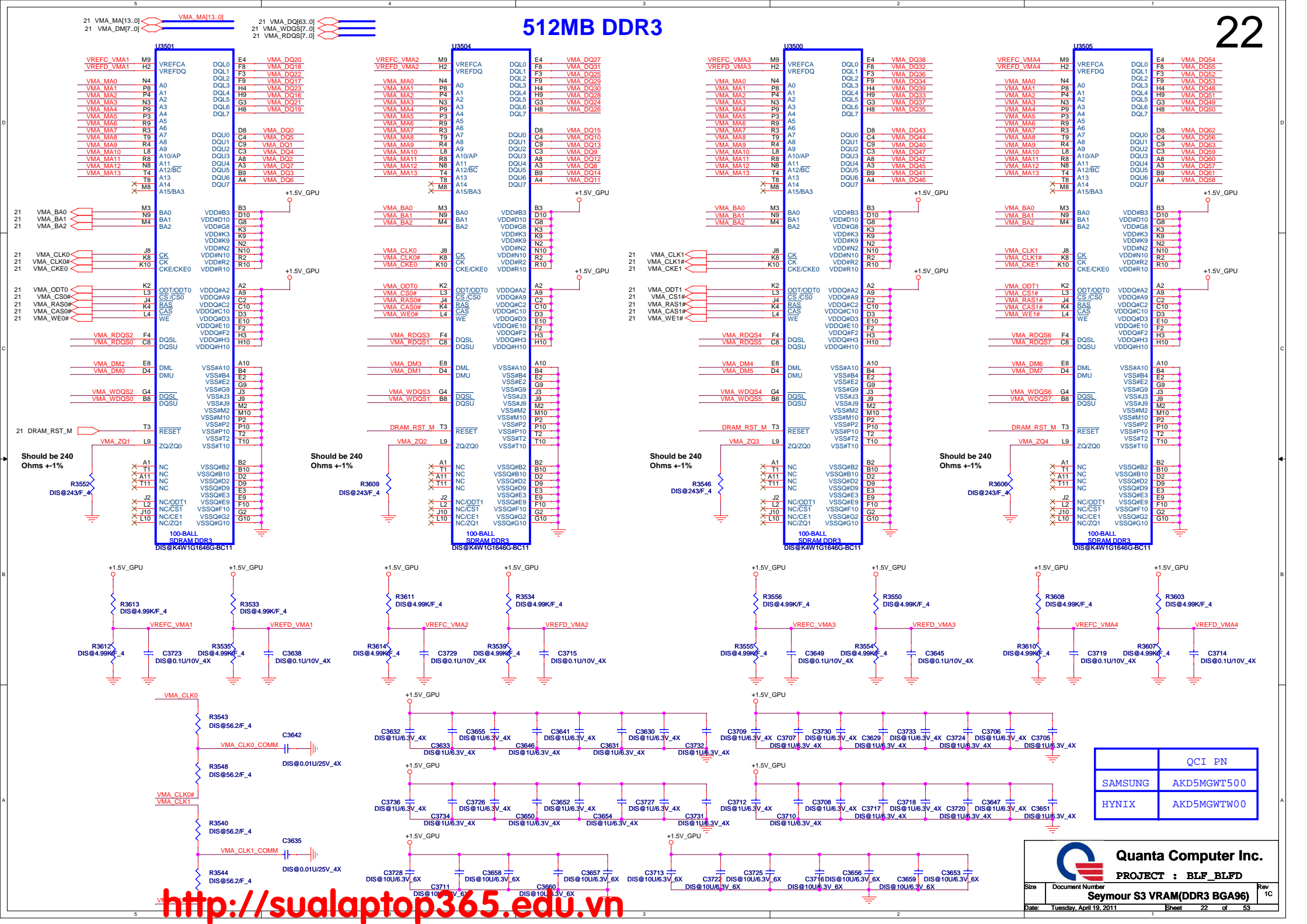
GDDR5 / DDR3

MEMORY INTERFACE



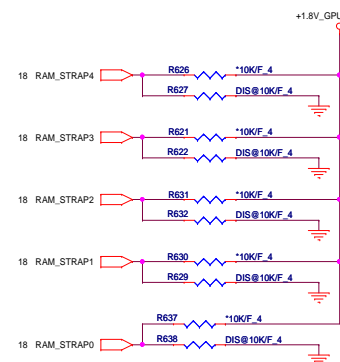
Designator	Robson
Ra	5K
Rb	10R
Ca	120pF
Rg	51R



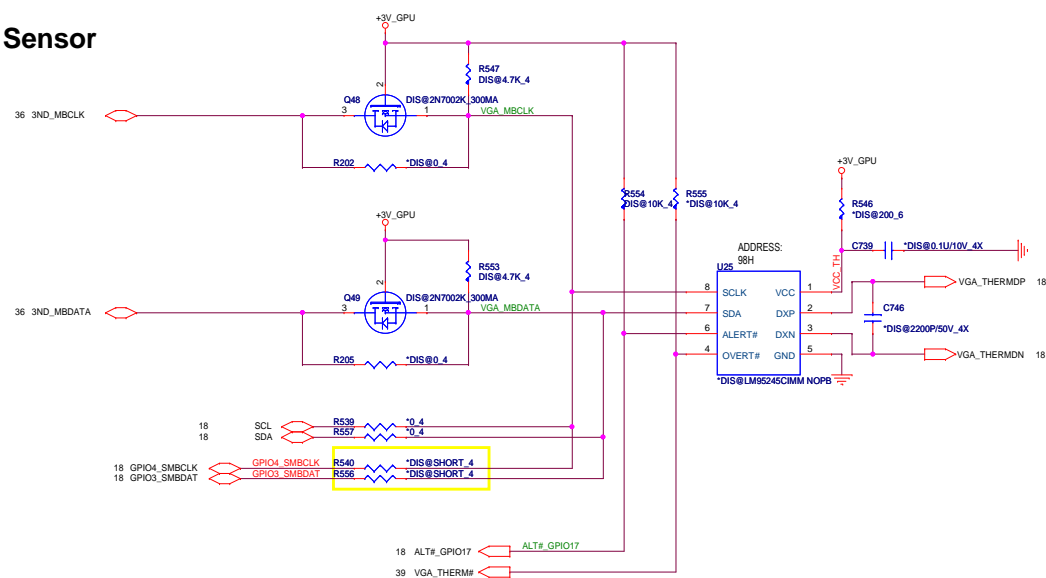


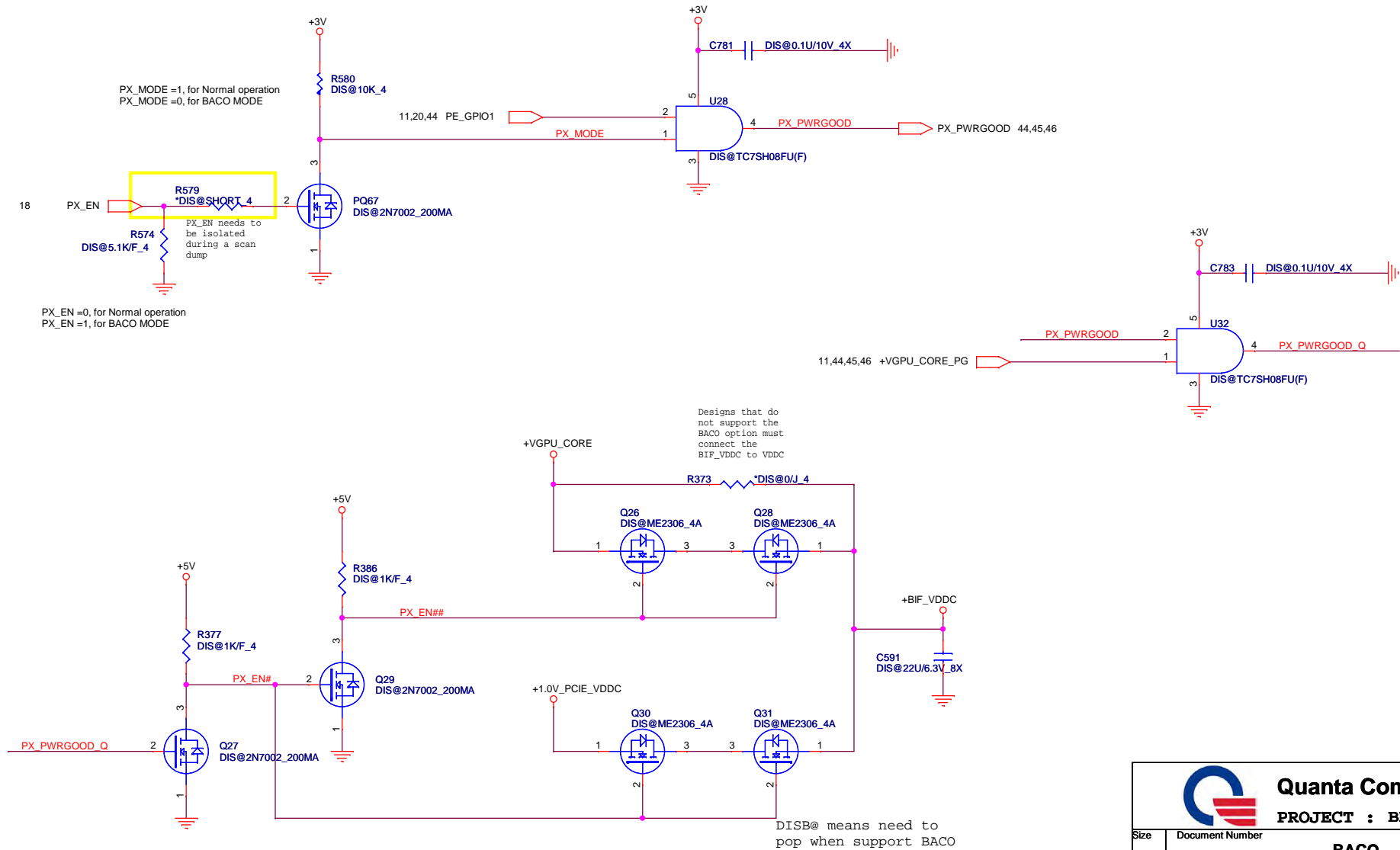
VRAM Memory TYPE


Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3	RAM_STRAP2	RAM_STRAP1	RAM_STRAP0	RAM_STRAP4	
				DVPDATA_3	DVPDATA_2	DVPDATA_1	DVPDATA_0	15"	14"
Hynix	H5TQ1G63DFR-11C	AKD5LZW7W02 (64M*16-1Gb)	512MB	0	1	0	0	0	1
	H5TQ2G63BFR-11C	AKD5MGWTW00 (128M*16-2Gb)	1GB	0	0	0	0	0	1
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	512MB	0	1	0	1	0	1
	K4W2G1646C-HC11	AKD5MGWWT500 (128M*16-2Gb)	1GB	0	0	0	1	0	1




Thermal Sensor

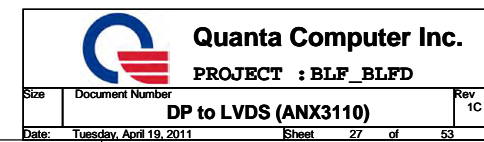




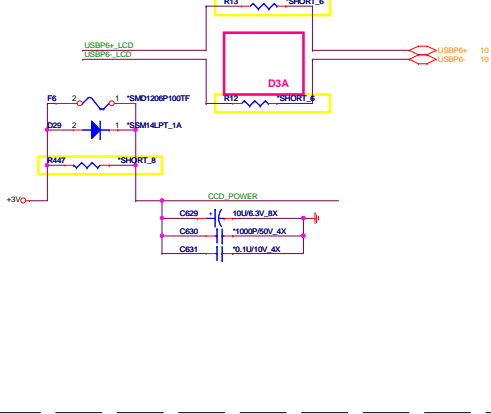
 Quanta Computer Inc. PROJECT : BLF_BLFD		Size	Document Number	Rev
				1C
Date:	Tuesday, April 19, 2011	Sheet	24 of 53	

 Quanta Computer Inc. PROJECT : BLF_BLFD		Rev 1C
Size	Document Number Blank	
Date:	Tuesday, April 19, 2011	Sheet 25 of 53



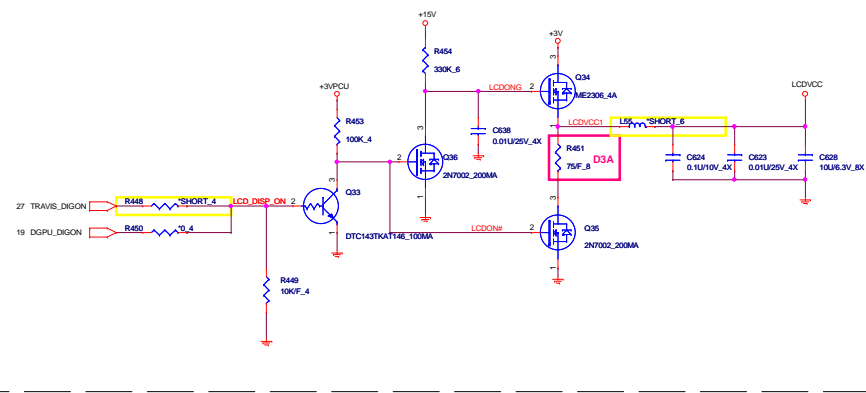


CCD [CCD]



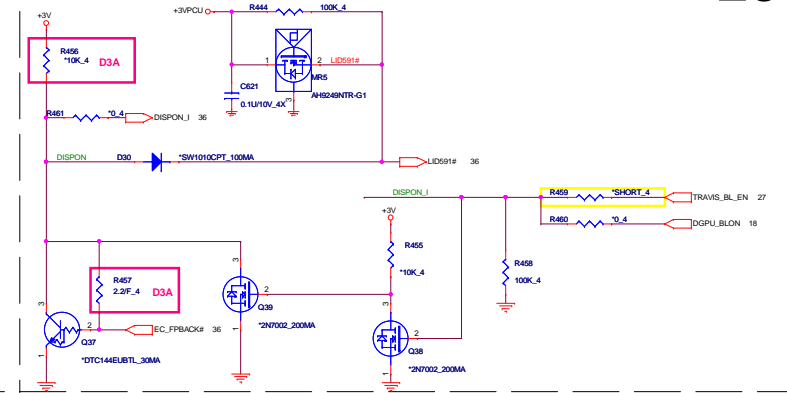
LCD POWER SWITCH

[LDS]



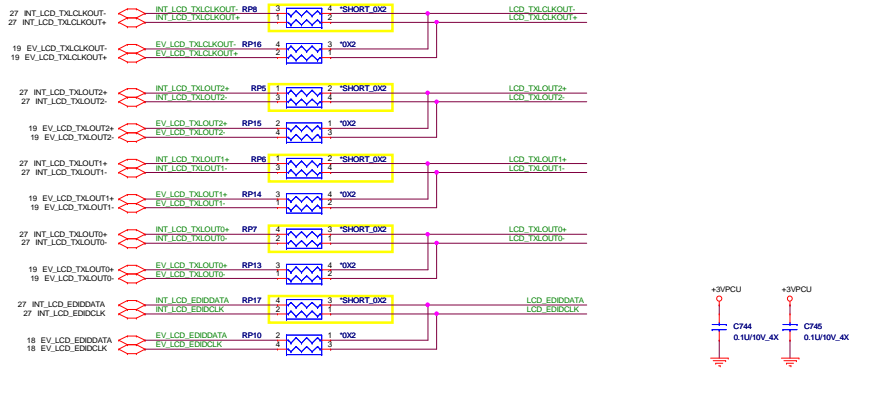
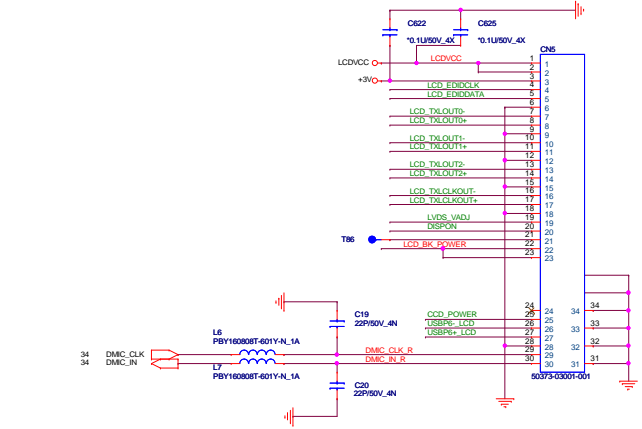
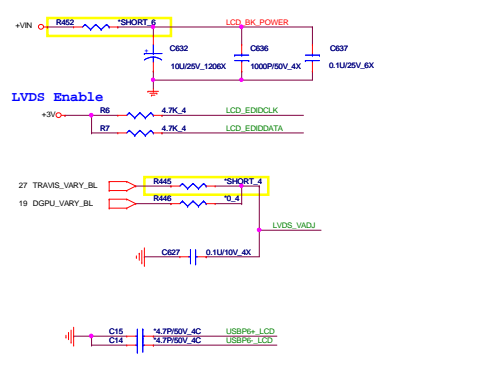
HALL SENSOR&BACK LIGHT SWITCH

[HSR]

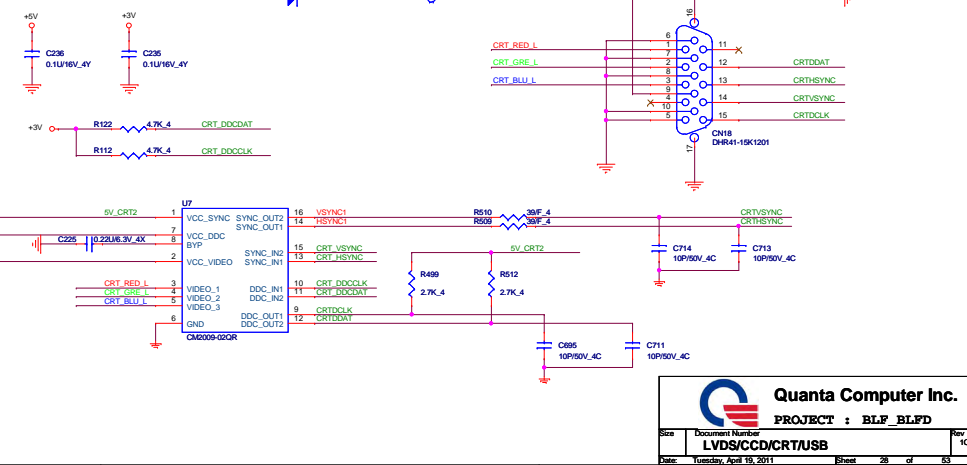
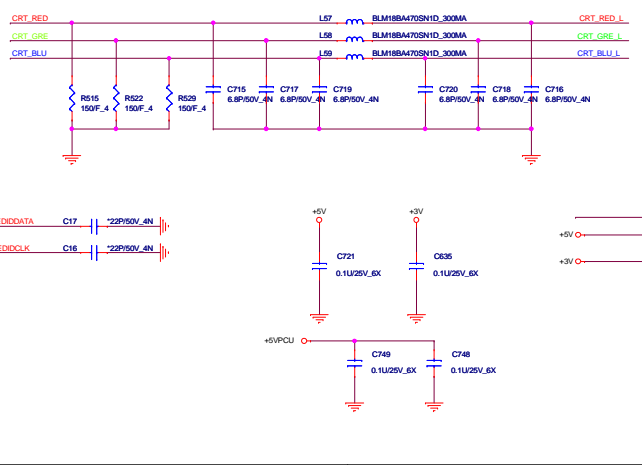
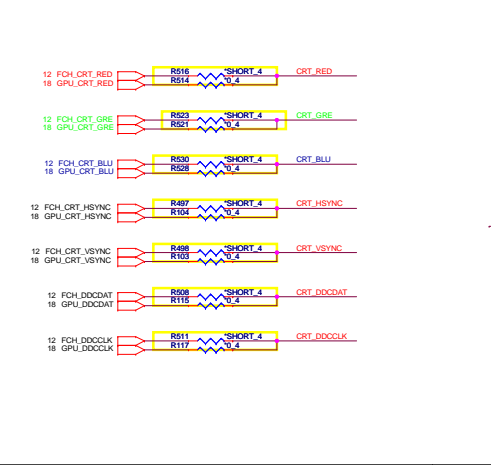


[LDS]

LCD Panel Module

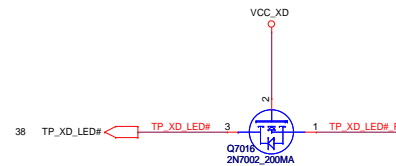
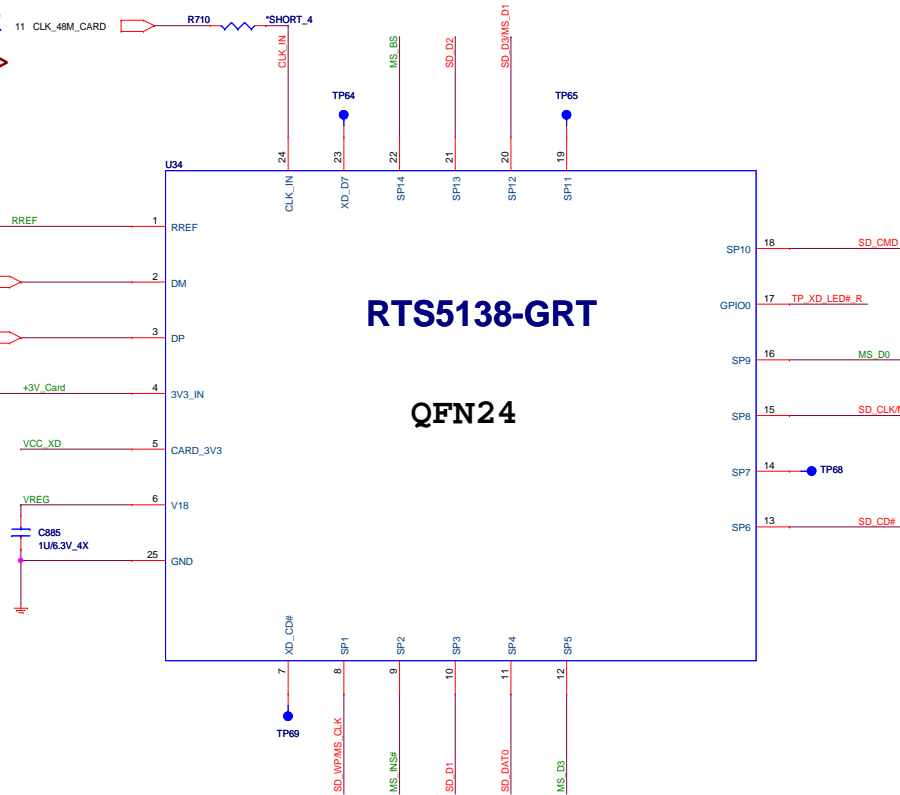


CRT [CRT]

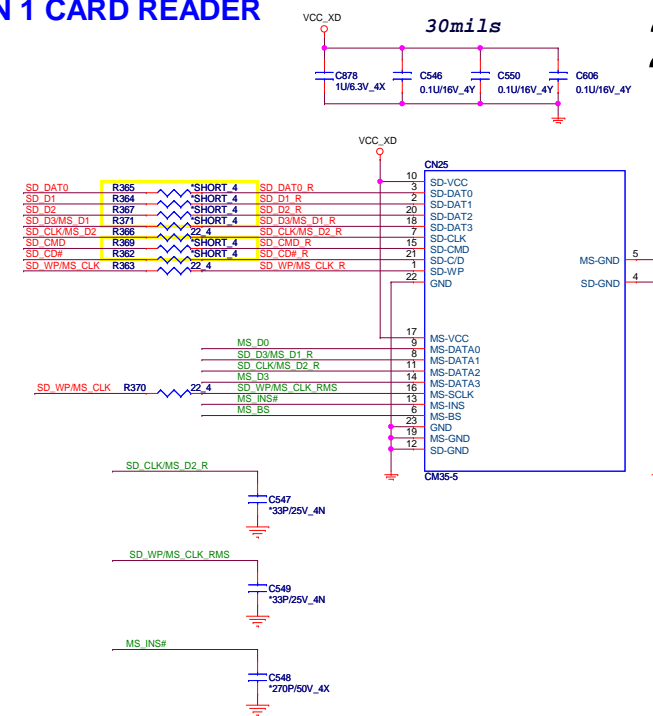


3 IN 1 CARD READER

Card reader controller <MMC>



3 IN 1 CARD READER

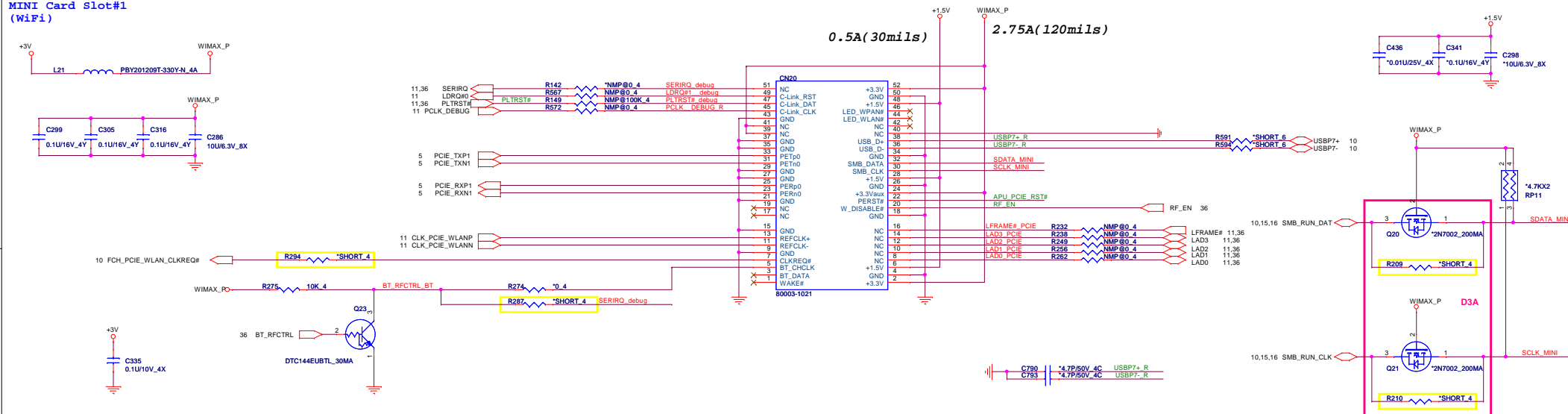


Quanta Computer Inc.

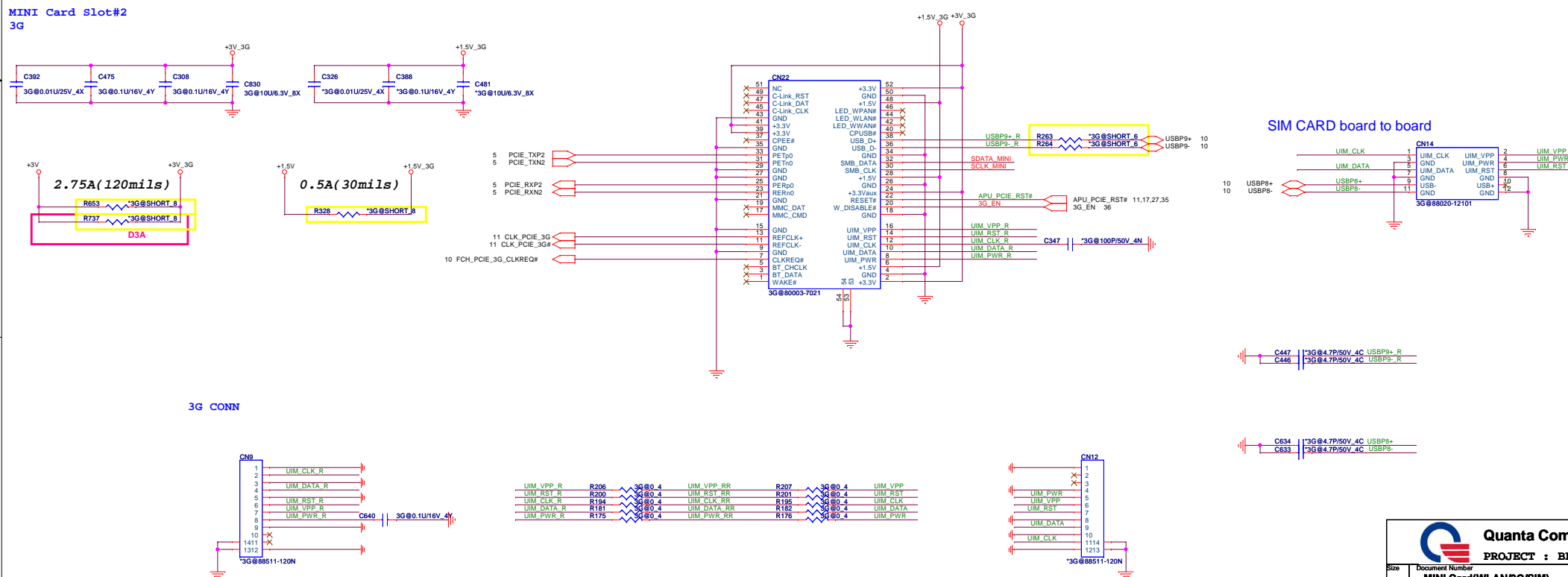
PROJECT : BLF_BFLD

Size	Document Number	Rev	1C
RTS5138 (Card Reader)			
Date: Tuesday, April 19, 2011		Sheet 29 of 53	

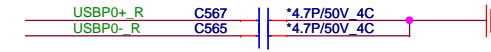
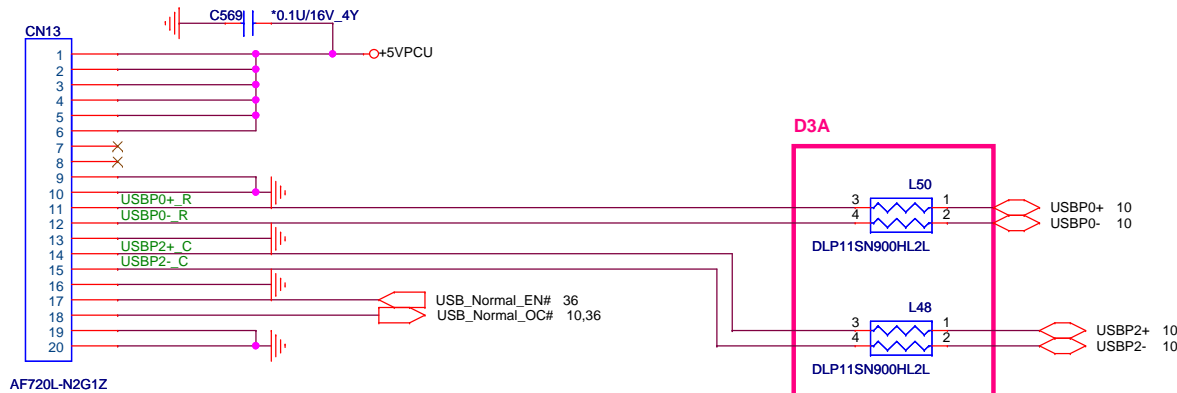
MINI Card Slot#1
(WiFi)



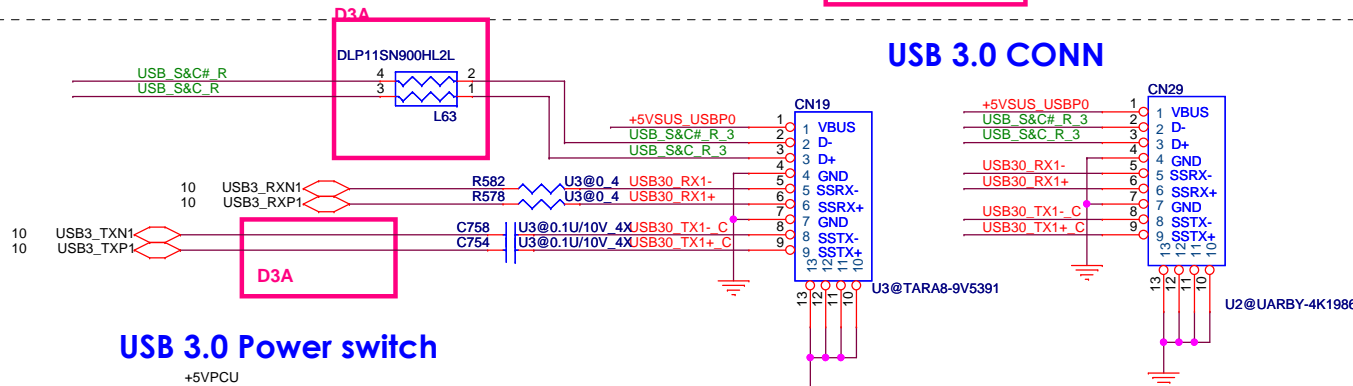
MINI Card Slot#2
3G



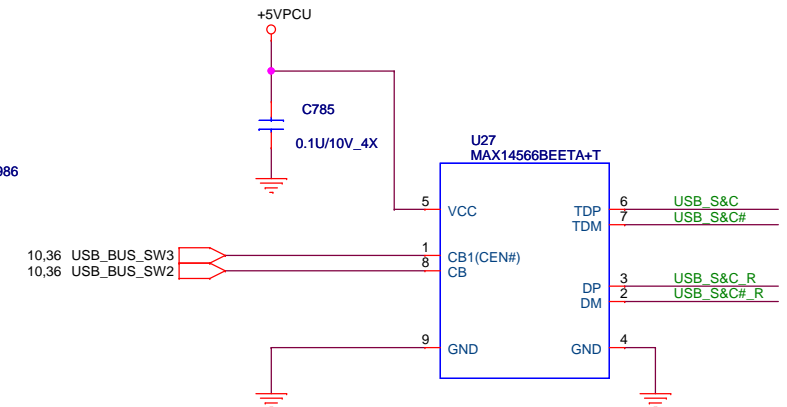
USB board



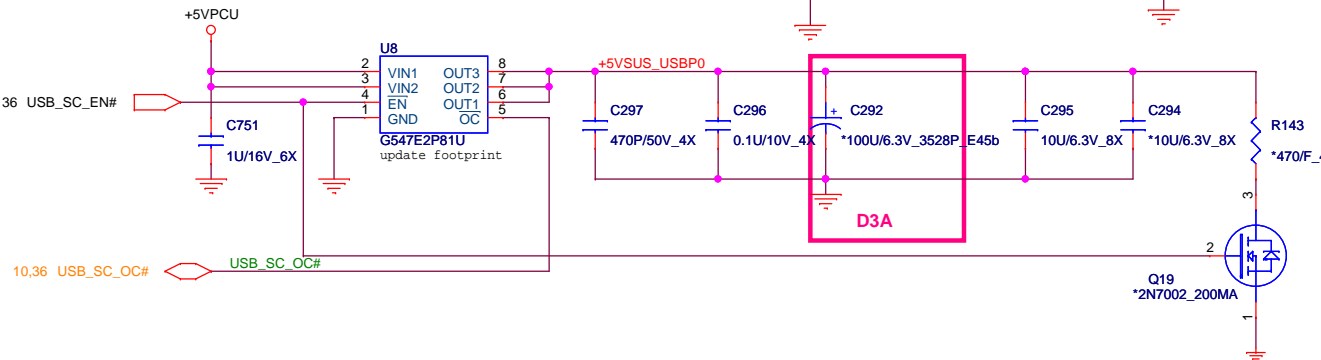
USB 3.0 CONN



USB Sleep & Charge MAXIM solution



USB 3.0 Power switch




CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

10 USB_S&C#
10 USB_S&C

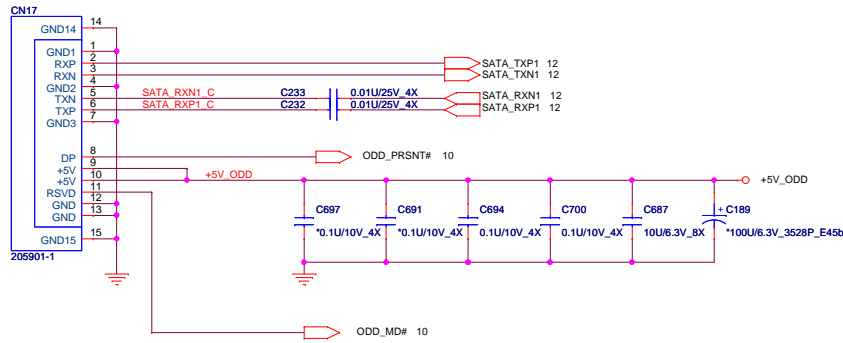
Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev 1C
USB2.0X1+USB3.0X1		
Date:	Tuesday, April 19, 2011	Sheet 31 of 53

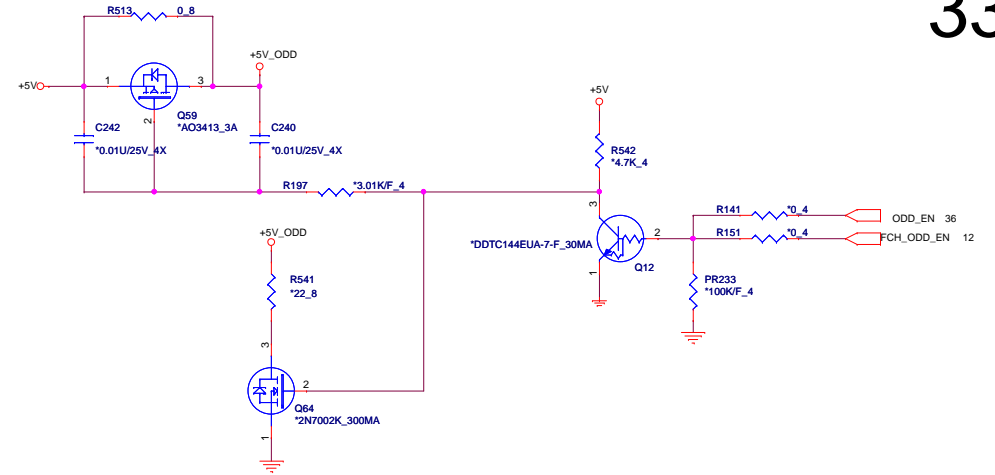
 Quanta Computer Inc. PROJECT : BLF_BLFD		Rev 1C
Size	Document Number BLANK	
Date:	Tuesday, April 19, 2011	Sheet 32 of 53

SATA ODD

[ODD]

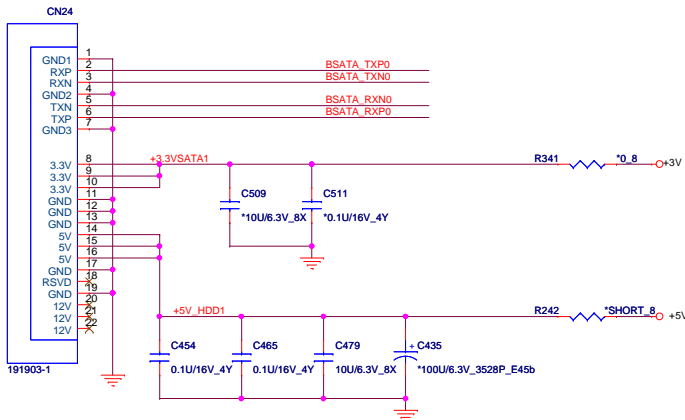


ODD Zero power .

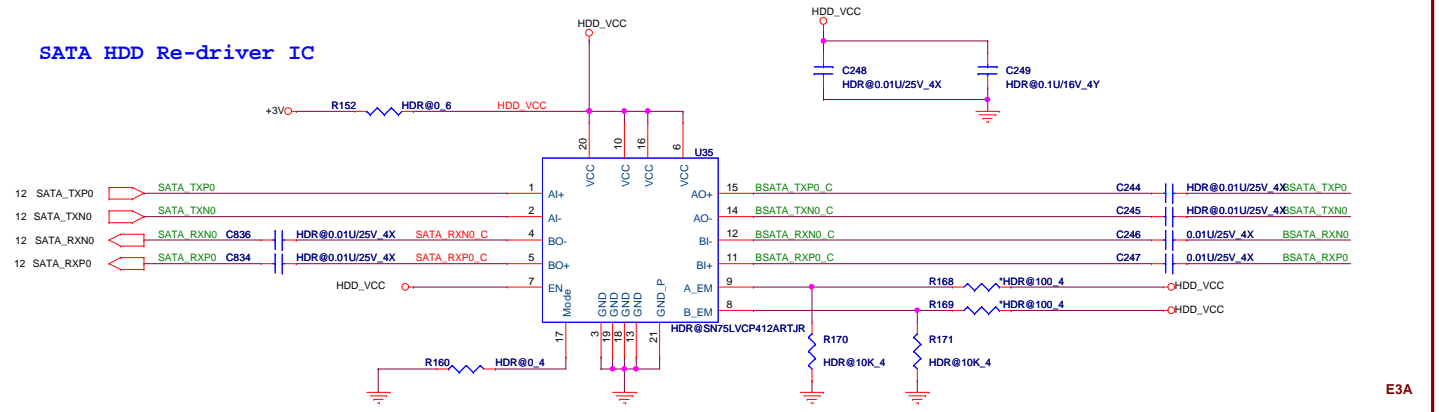


SATA HDD

[HDD]



SATA HDD Re-driver IC



Colay with Redriver IC SATA Re-driver Bypass

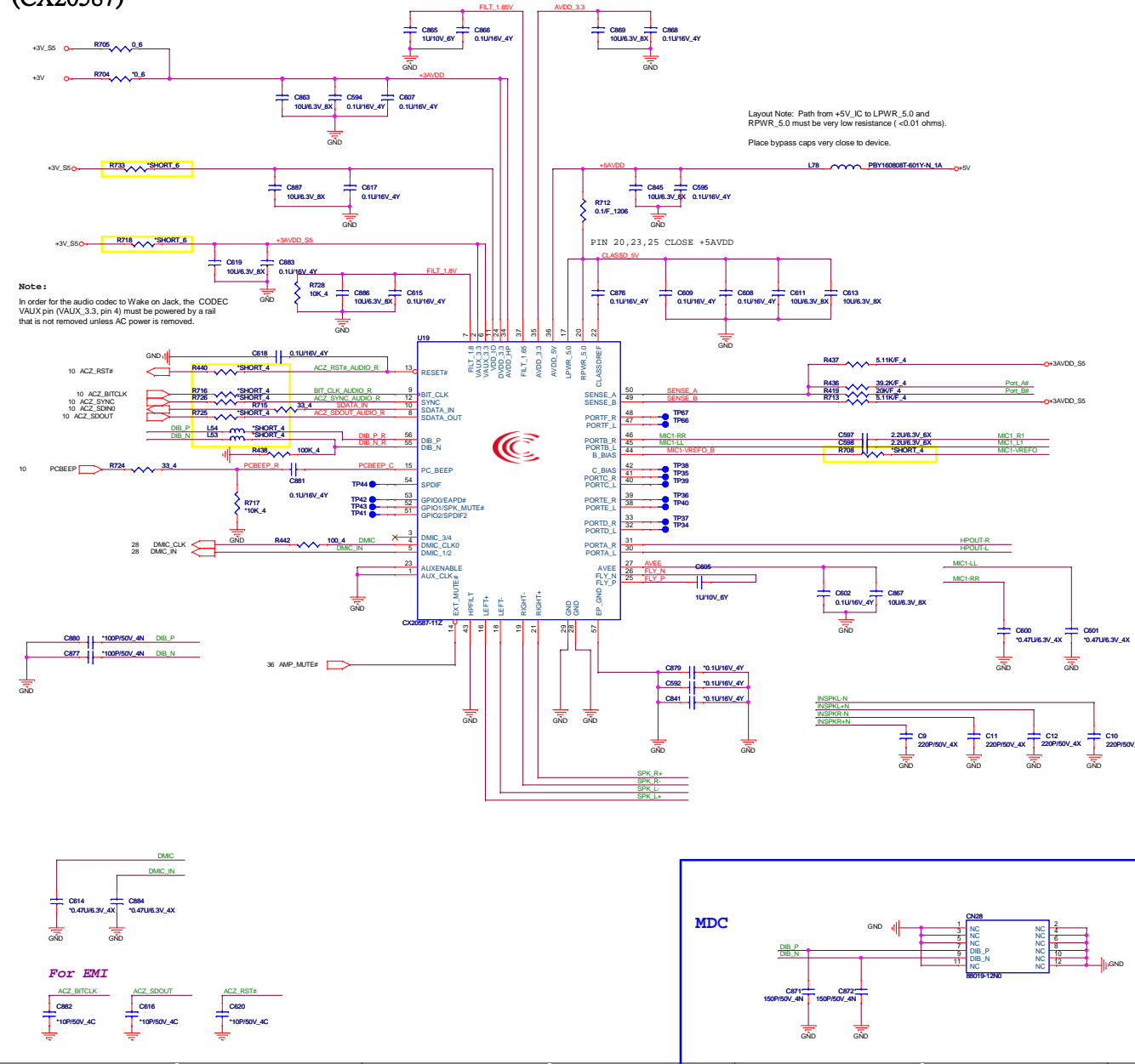
SATA_TXP0	R164	*0.4	BSATA_TXP0
SATA_TXN0	R165	*0.4	BSATA_TXN0
SATA_RXN0	R166	*0.4	BSATA_RXN0_C
SATA_RXP0	R167	*0.4	BSATA_RXP0_C

E3A

Quanta Computer Inc.
PROJECT : BLF_BLFD

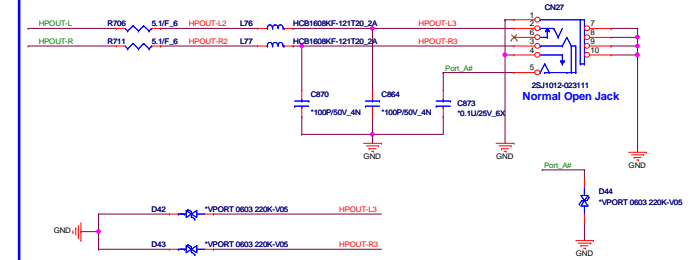
Size: Document Number
HDD/ODD/MDC
Date: Tuesday, April 19, 2011
Sheet: 33 of 53
Rev: 1C

Codec (CX20587)

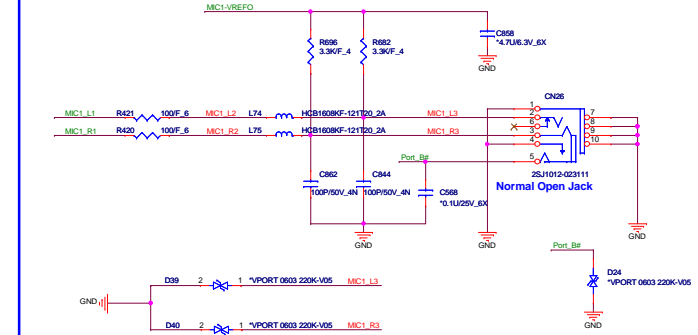


34

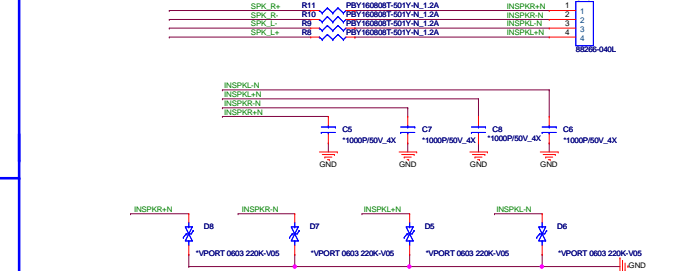
Earphone



External MIC

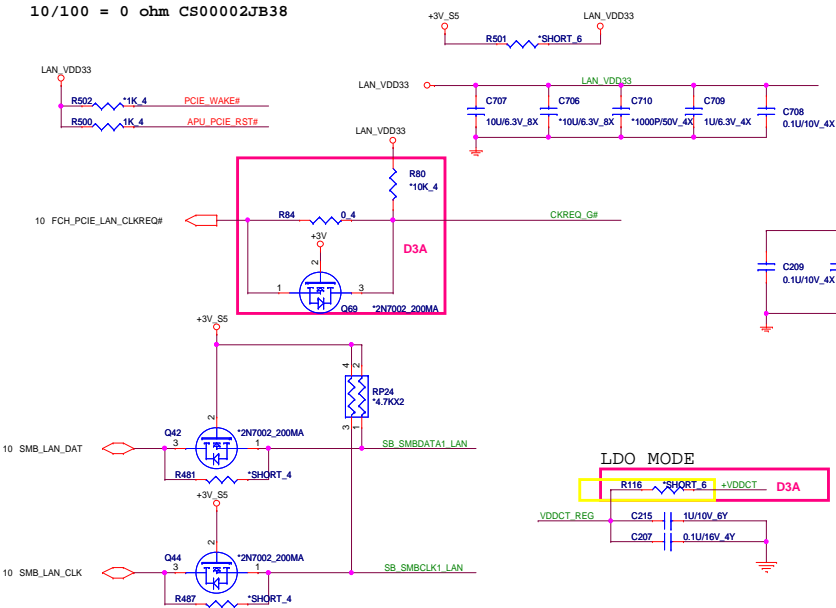


Internal Speaker

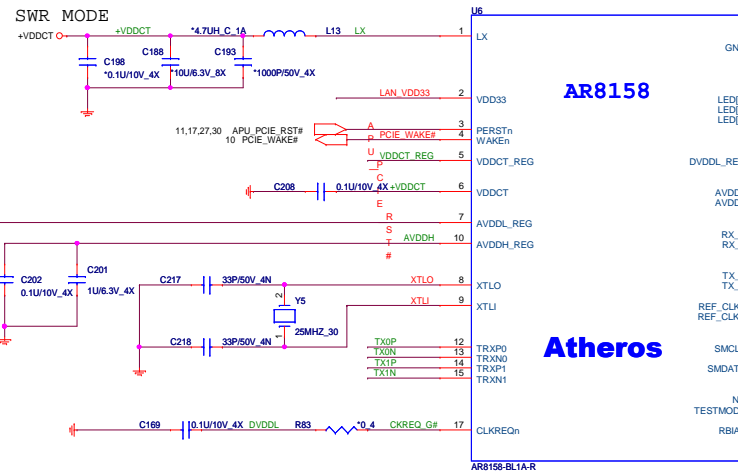
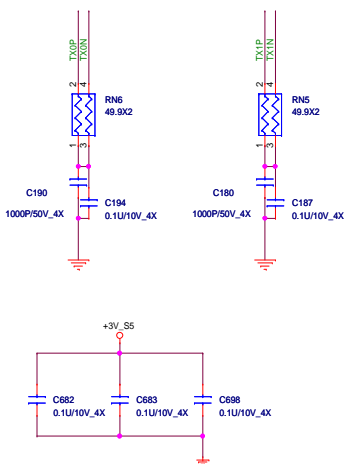


Atheros Lan AR8158

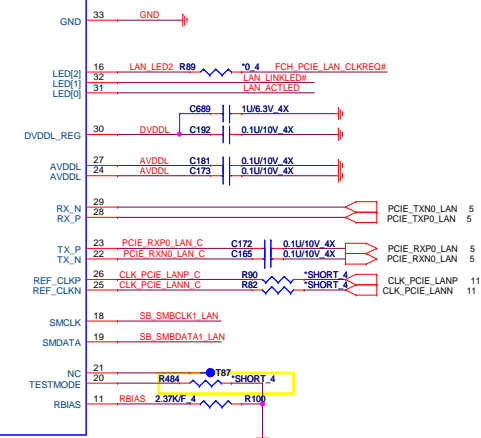
10/100 = 0 ohm CS00002JB38



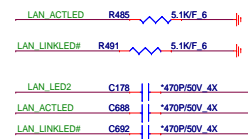
PLACE NEAR LAN IC SIDE



AMD 10/100: AR8158-BL1A-R = AL008158001

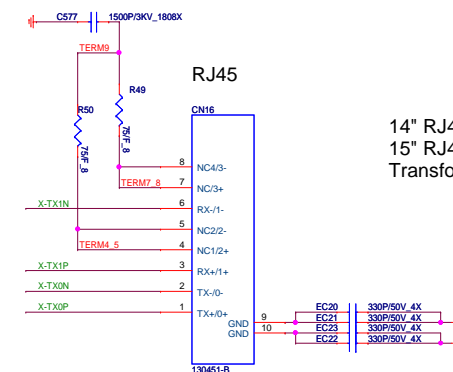
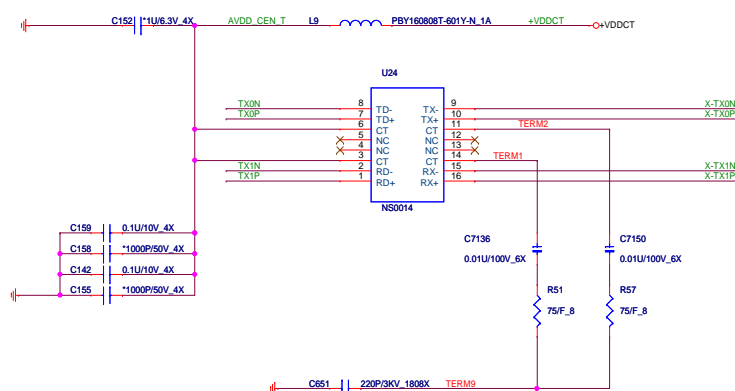


Power on Strapping pin

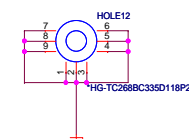


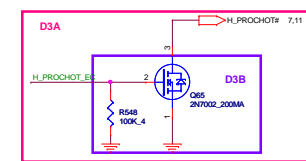
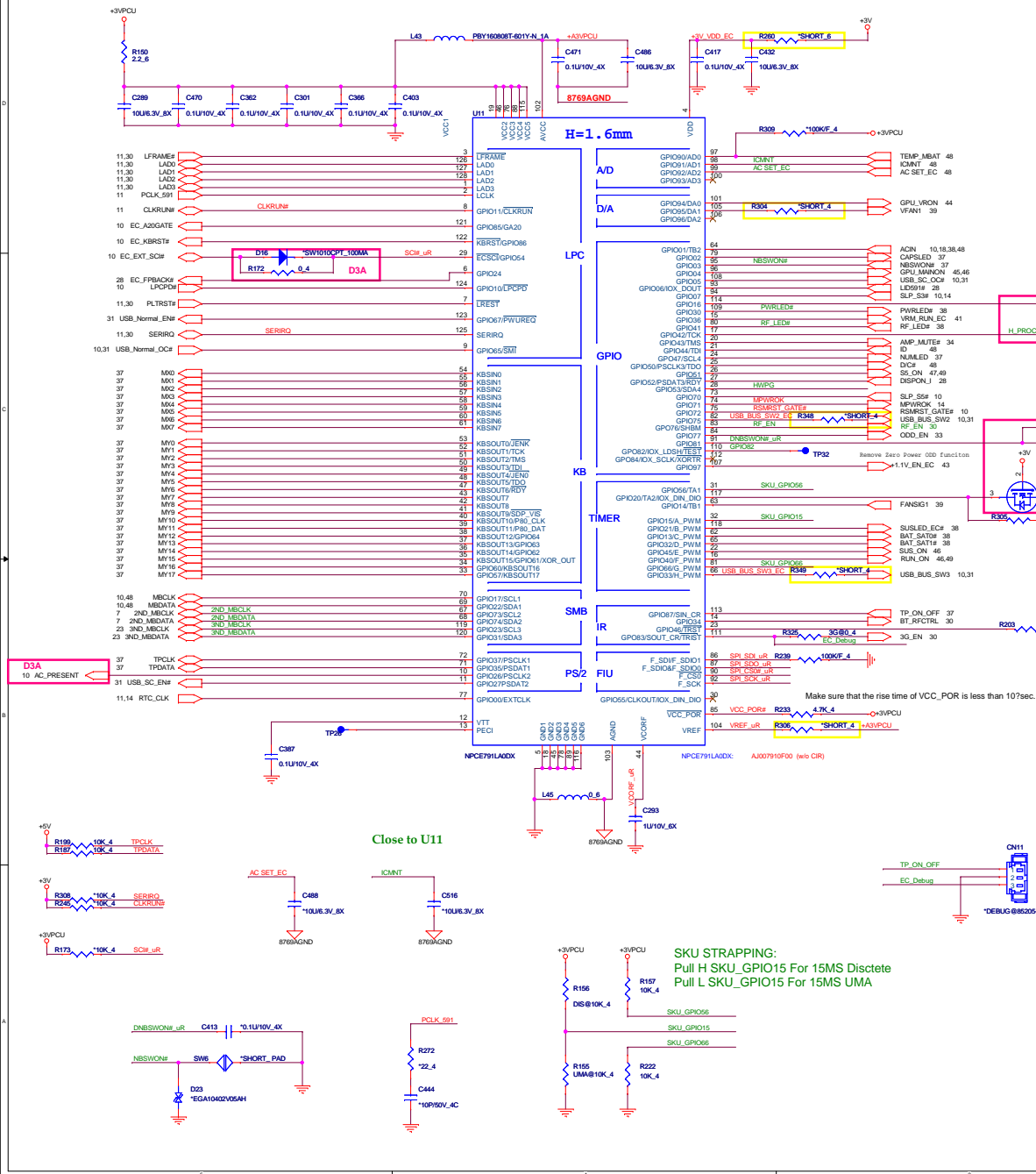
LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low

TRANSFORMER

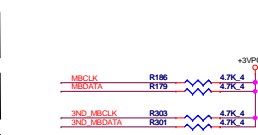


14" RJ45- DFTJ08FR164
15" RJ45- DFTJ08FR169
Transformer- DB0EL5LAN02





SM BUS PU



SMBUS Table

1	Devices	Address
2	Battery	
3	PCH SML1 3D Sensor	32H
	EC EEPROM	A0H
	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	53H

Strap



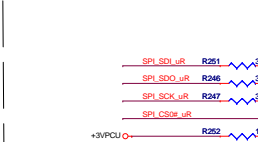
SHBM-I: Enable shared memory with host BIOS
 Disabled (T) if using FWH device on LPC
 Enabled (D) if using SPI flash for both system BIOS and EC firmware

ID EEPROM



0.003A (20m1s)

SPI FLASH

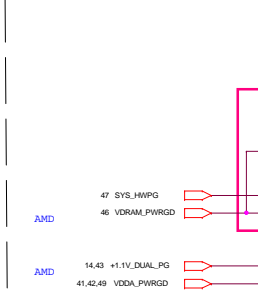


MX25L3205DM2I-12G: AKE39FP0200
 W25Q16BVSS1G: AKE38FP0N01

INTERNAL KEYBOARD STRIP SET

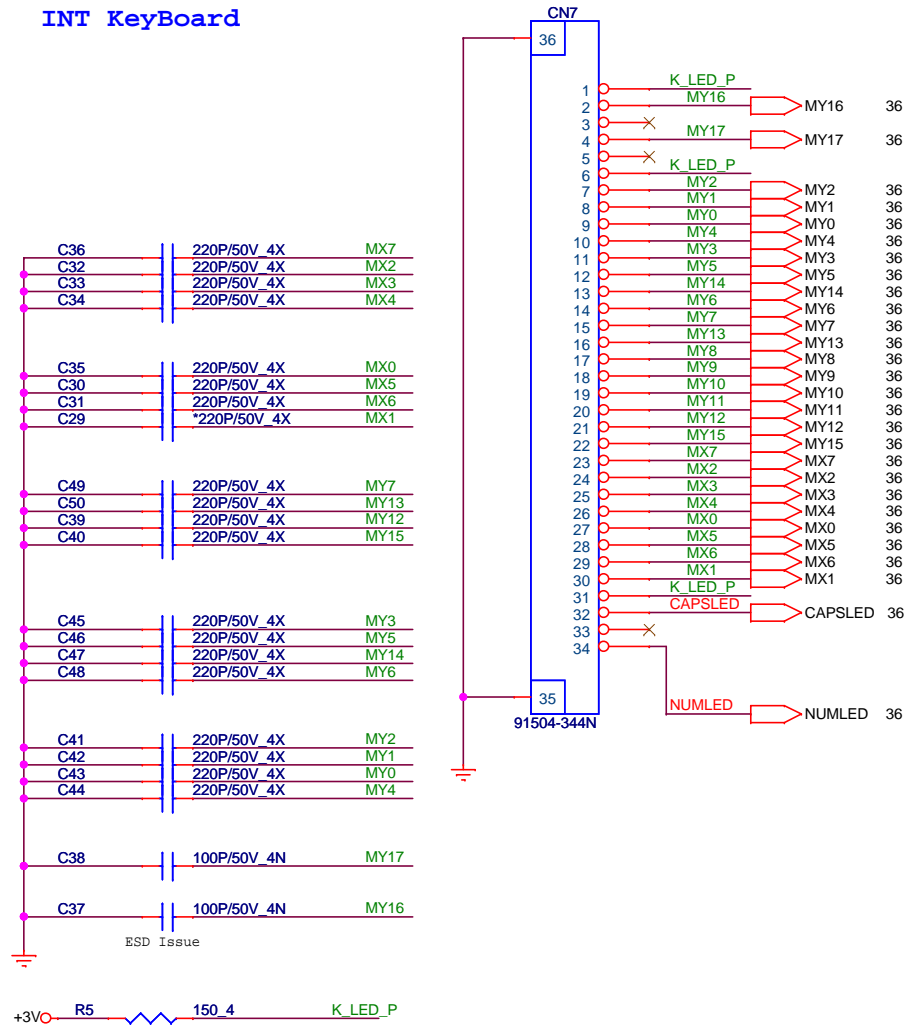


HWPG circuit



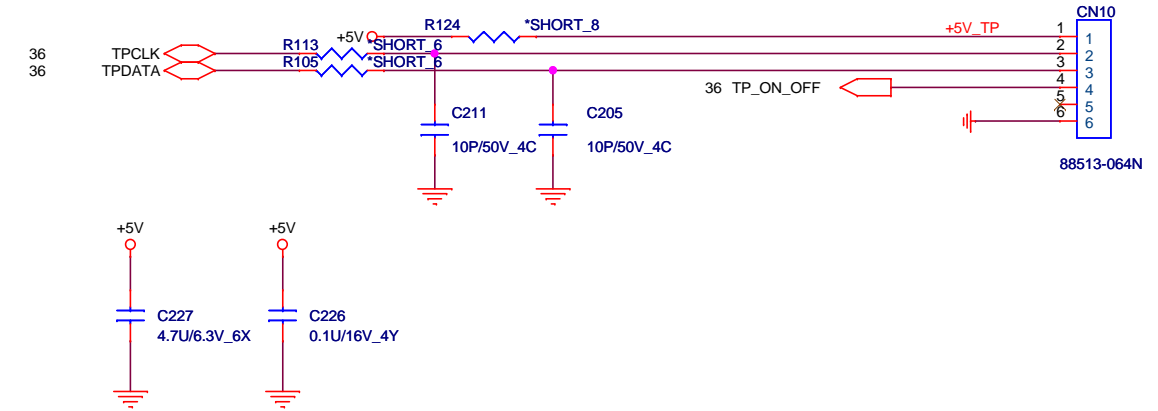
KEY BOARD Connector

INT KeyBoard

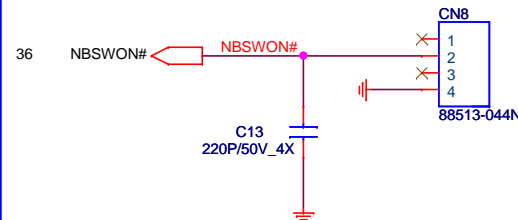


TOUCH PAD BOARD

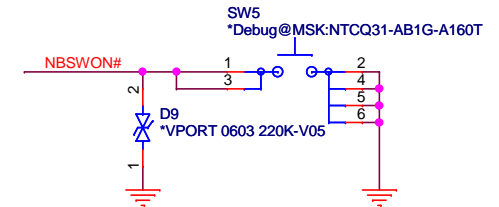
37



Power Board (UIF)



Power Switch (debug only)



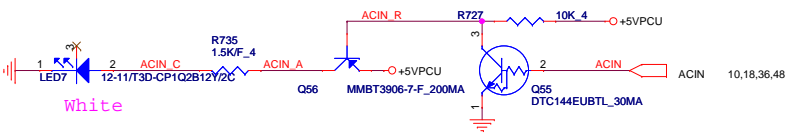
Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	FP/TP/KB Conn	1C
Date:	Tuesday, April 19, 2011	Sheet 37 of 53

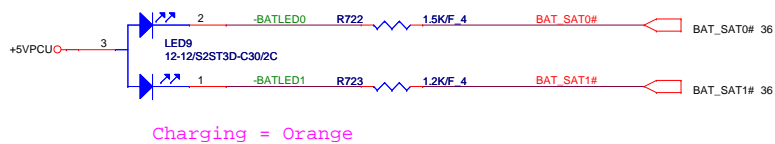
LED

AC-IN

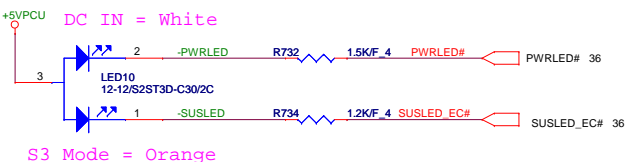


BATTERY

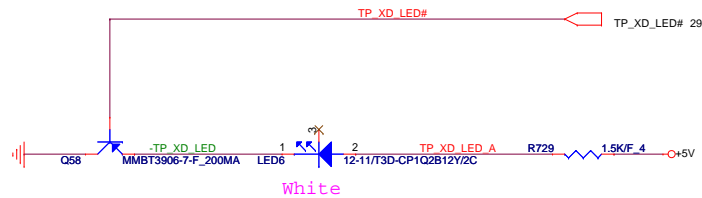
Full Charge = White



POWER

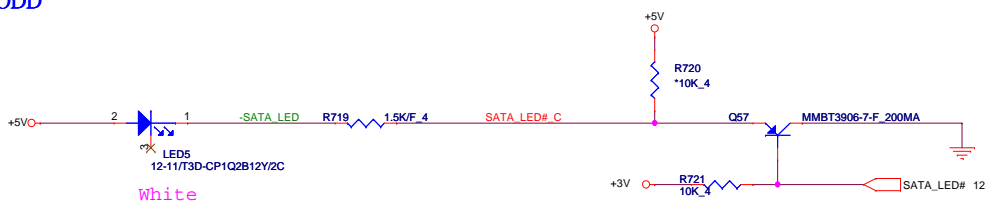
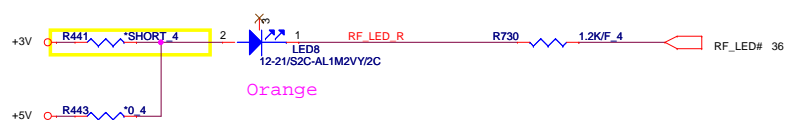


CARDREADER

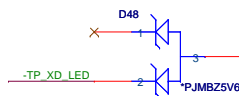
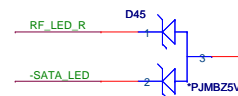
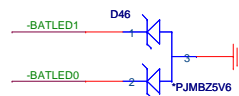
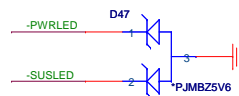


HDD/ODD

RF LED



When ON, means in S0
When BLINK, means in S3
When OFF, means in S5

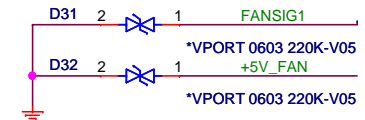
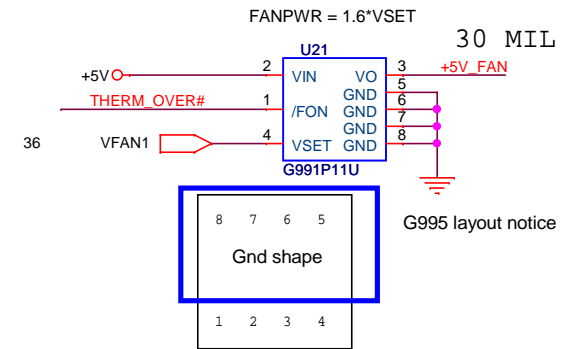
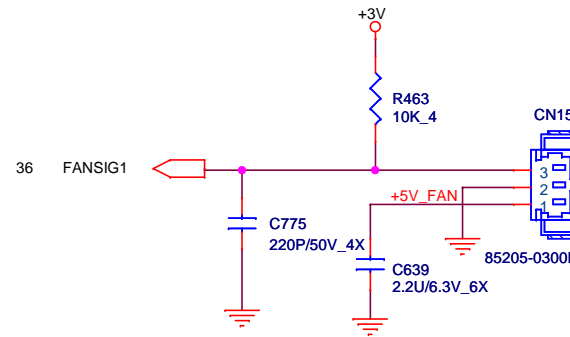
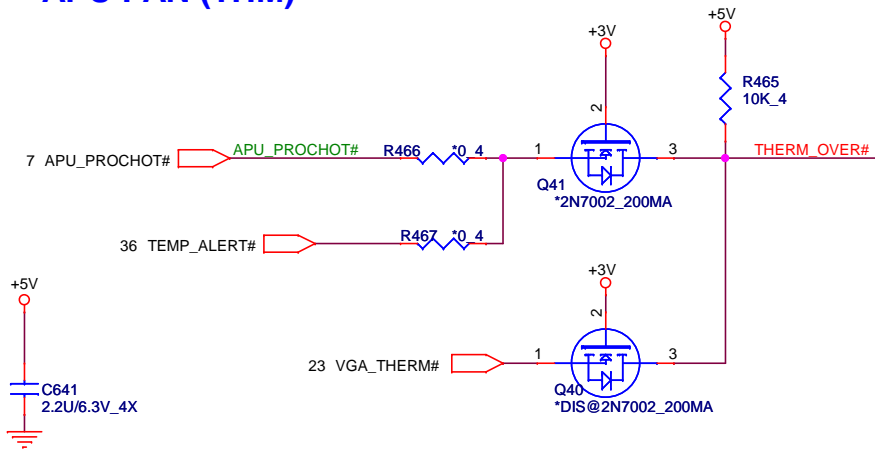


Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	LED	1C
Date: Tuesday, April 19, 2011	Sheet 38 of 53	

APU FAN (THM)

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Quanta Computer Inc.

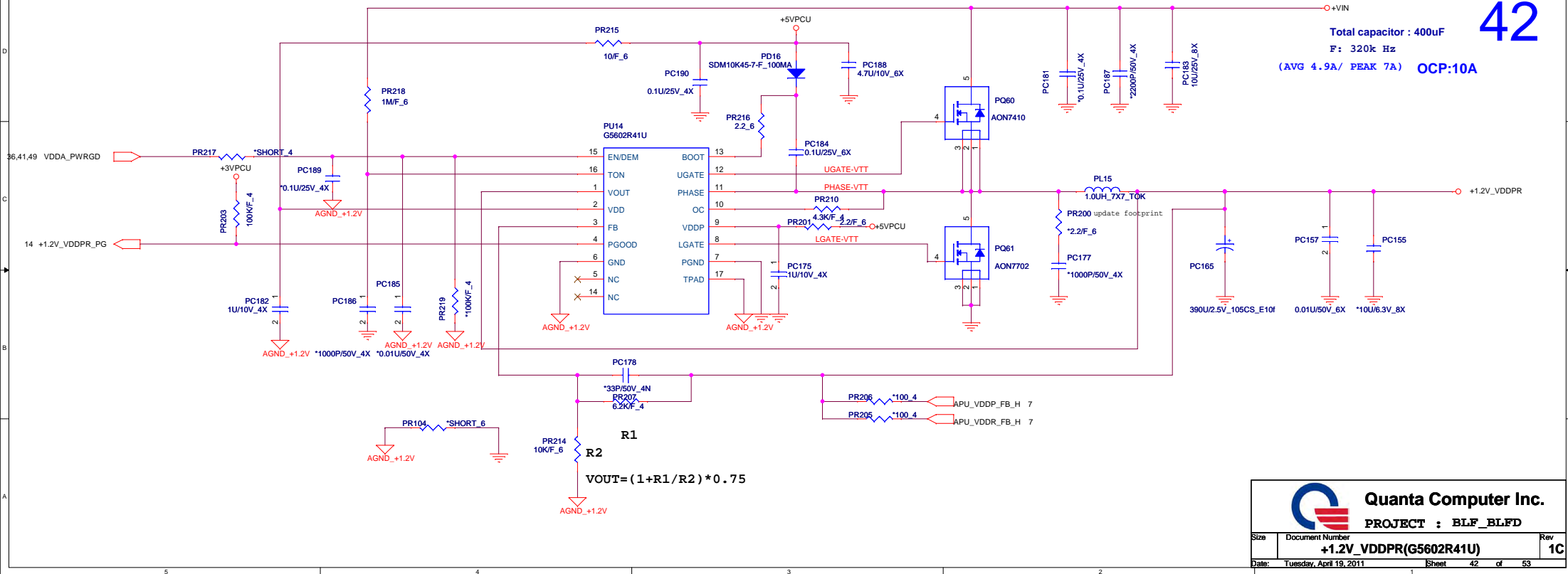
PROJECT : BLF_BLFD

Size	Document Number	Rev
	BLANK	1C
Date:	Tuesday, April 19, 2011	Sheet 40 of 53

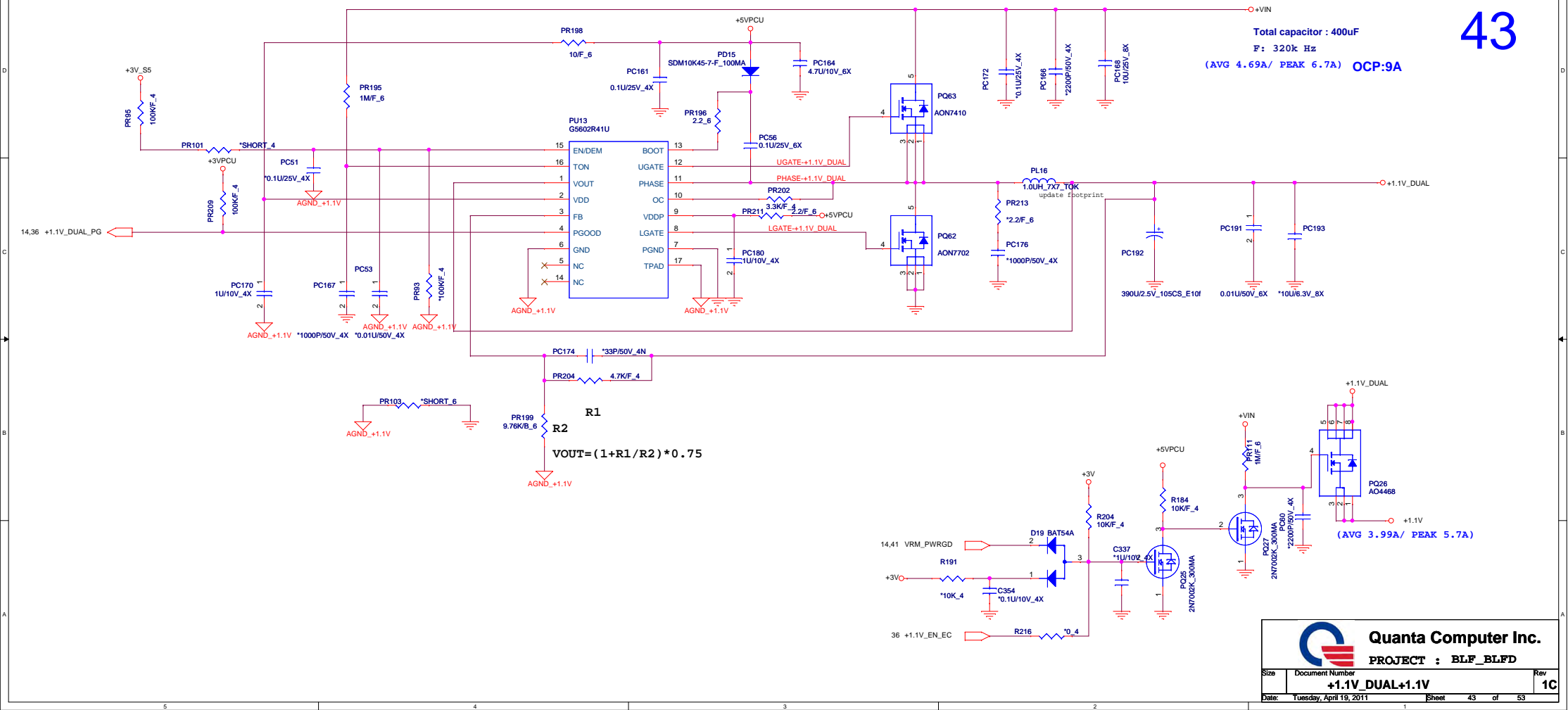


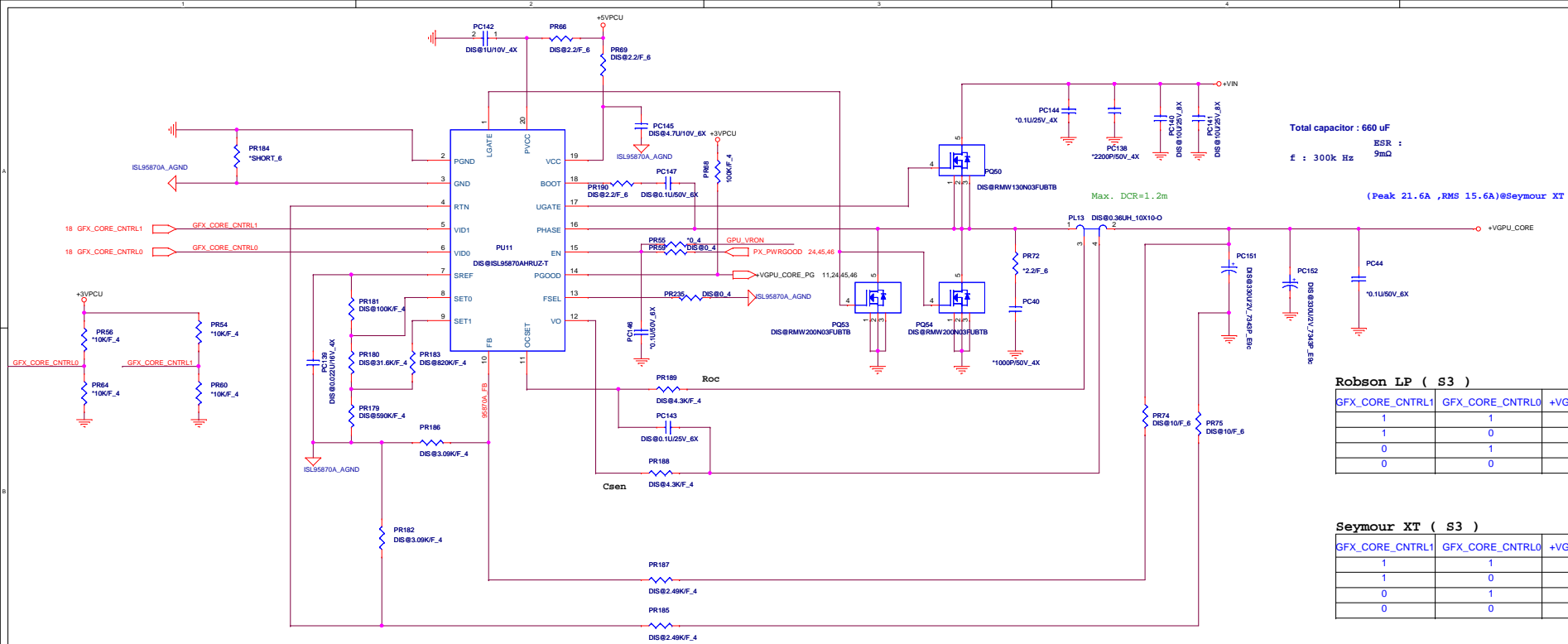
 <div> Quanta Computer Inc PROJECT : BLF_BLFD </div>	
Size	Document Number
CPU CORE	
Part No.	Quantity

Total capacitor : 400uF
F: 320k Hz
(AVG 4.9A/ PEAK 7A) OCP:10A



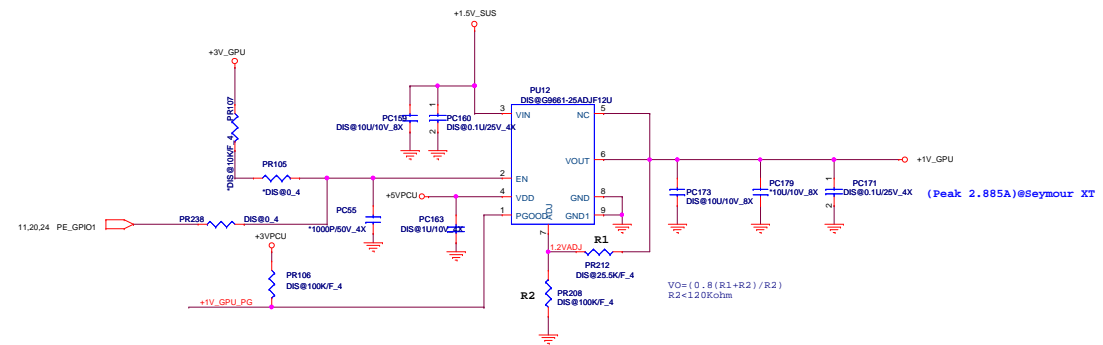
Total capacitor : 400uF
F: 320k Hz
(AVG 4.69A/ PEAK 6.7A) **OCP:9A**



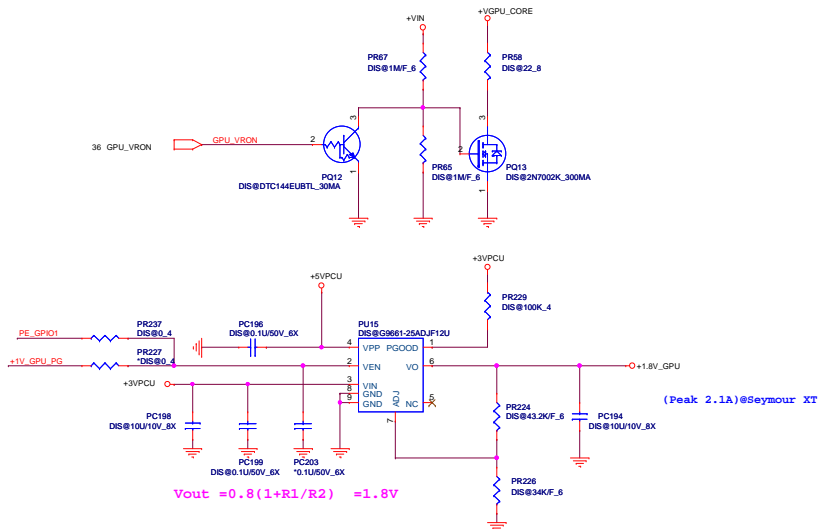


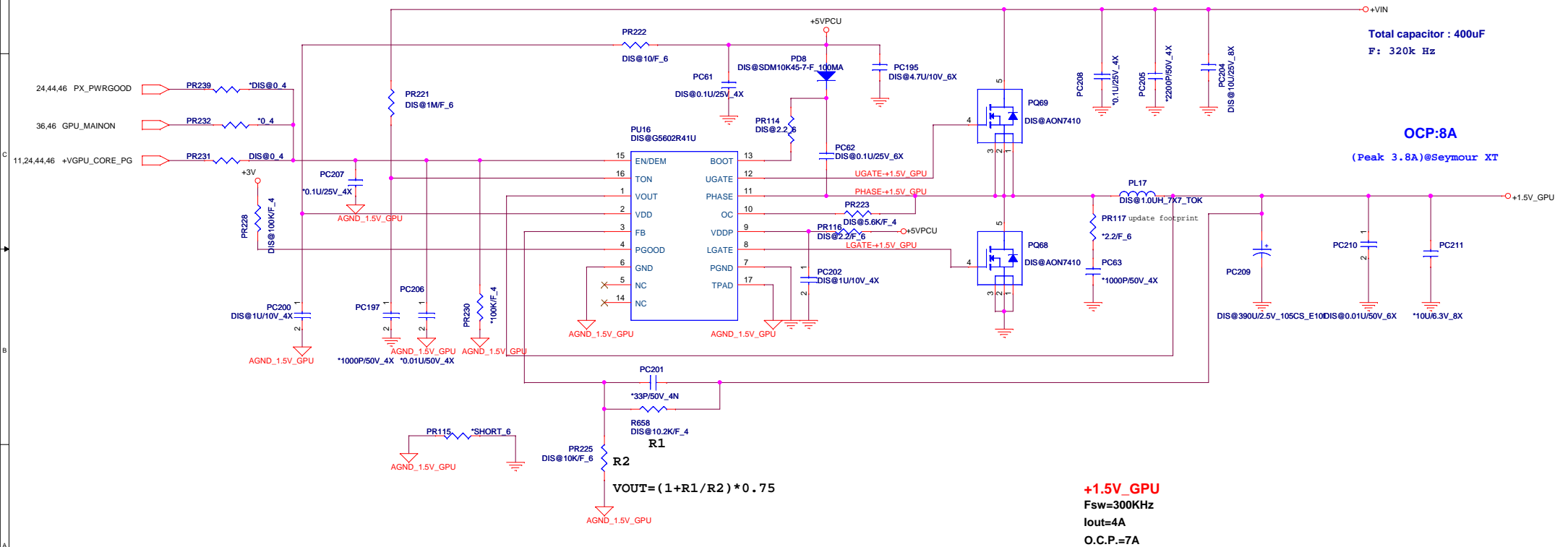
Robson LP (S3)		
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.12V


Seymour XT (S3)		
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	1.05V
0	1	1.1V
0	0	1.15V

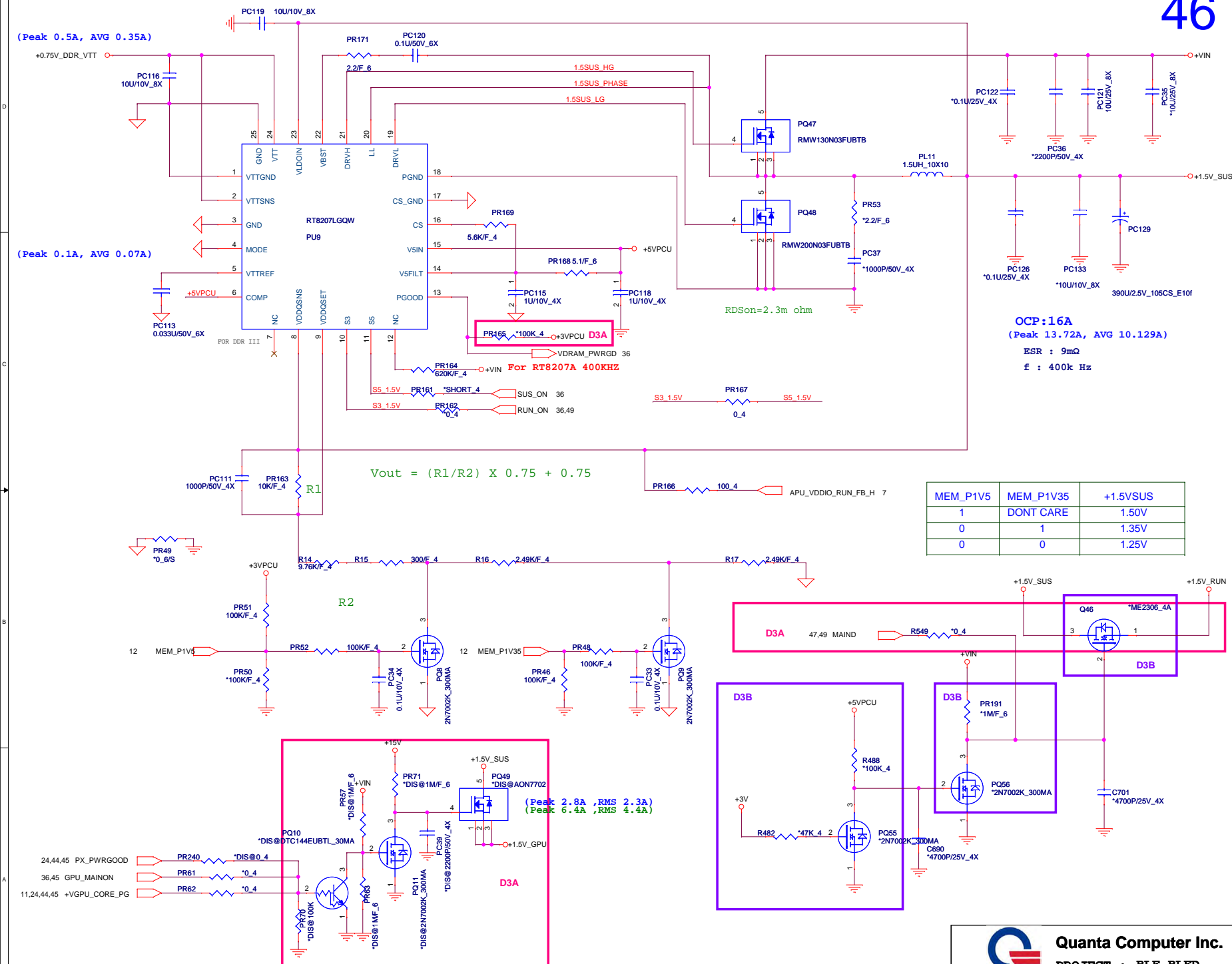
PCIE_VDDC
Madison,Park-->1.0V

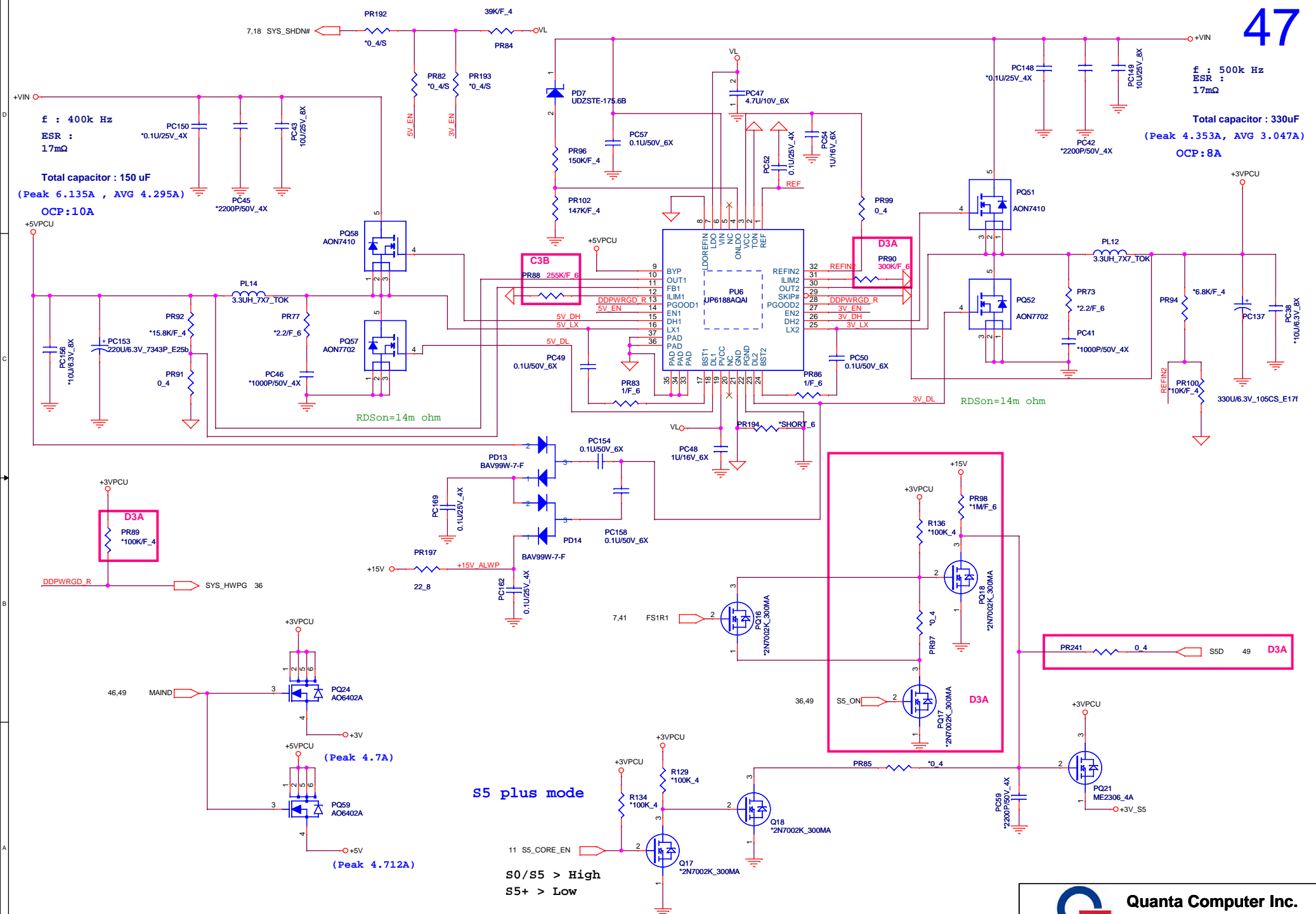
	Madison, Park
R1	25.5K/F_4 (CS32552FB11)
R2	100K/F_4 (CS41002FB28)

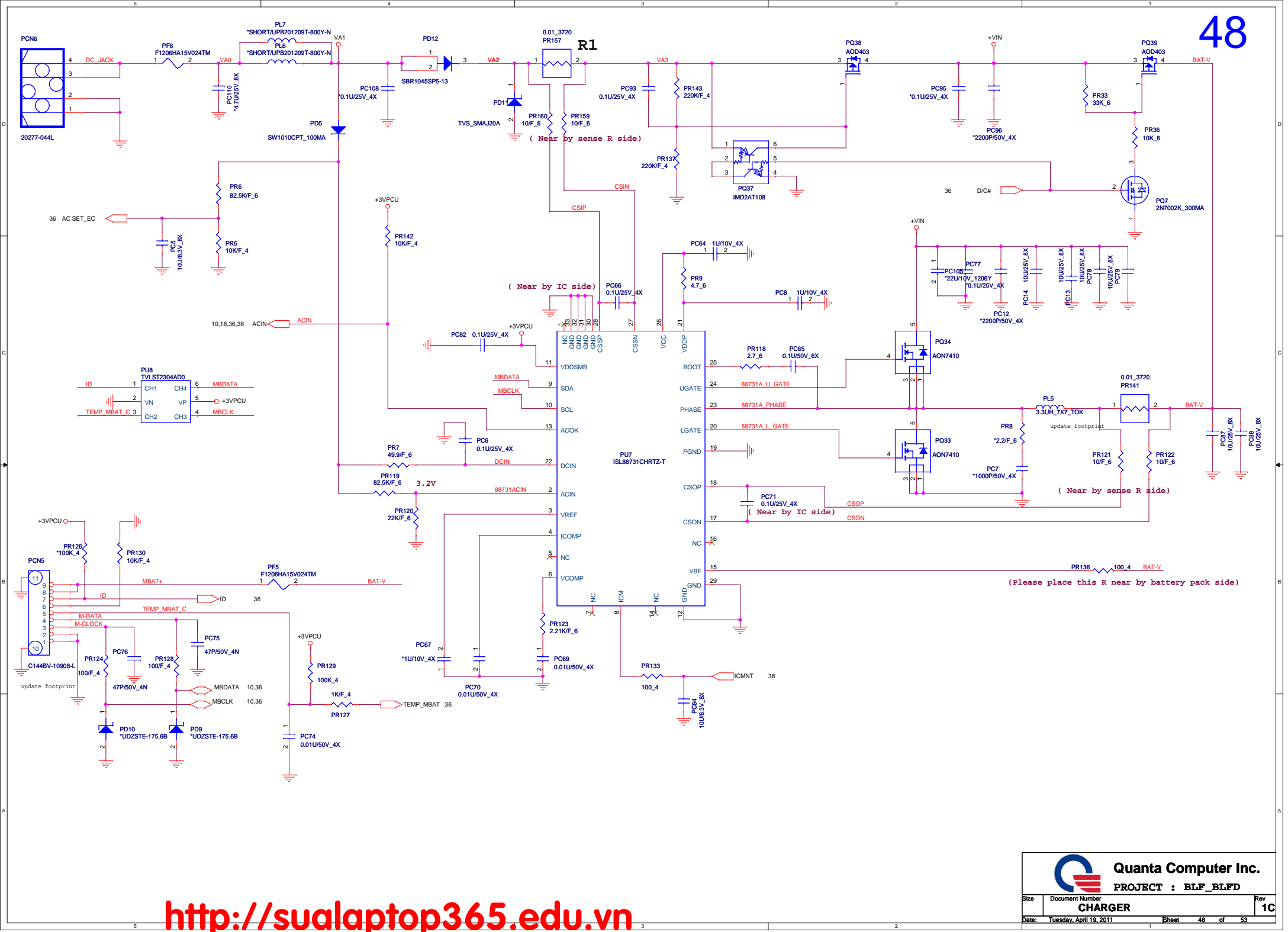




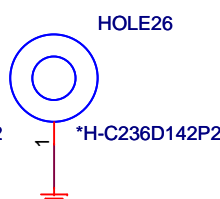
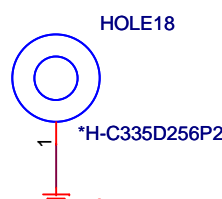
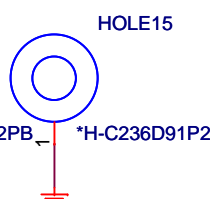
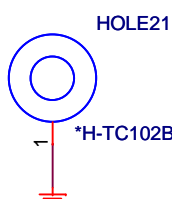
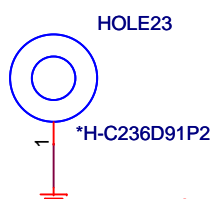
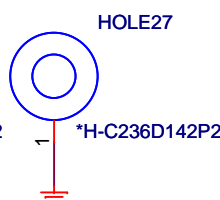
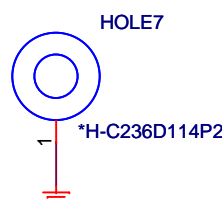
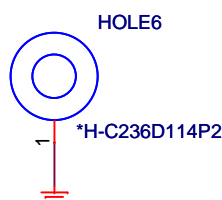
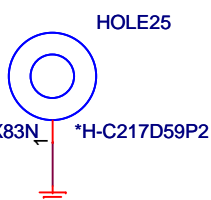
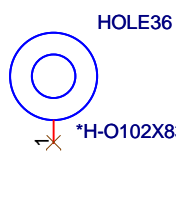
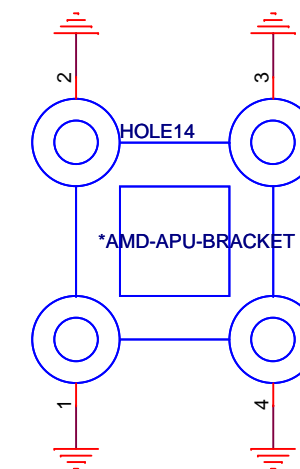
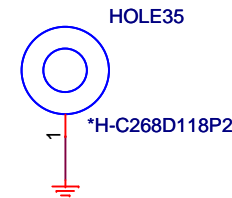
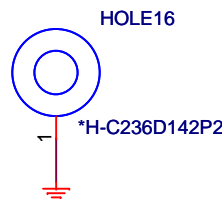
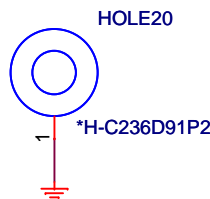
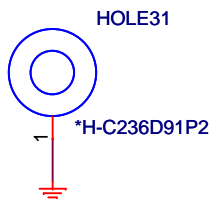
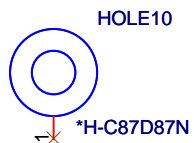
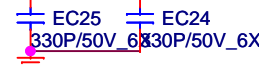
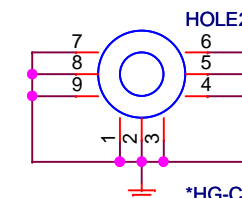
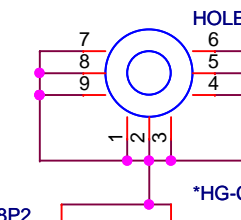
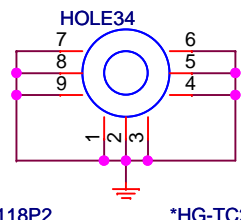
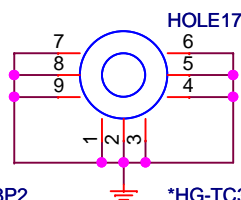
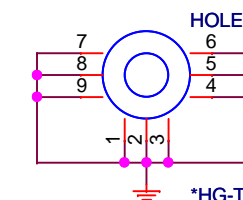
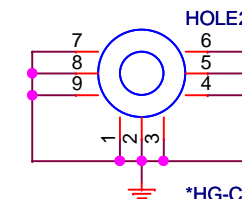
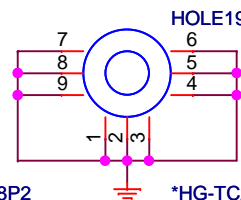
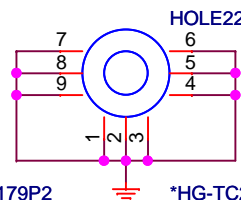
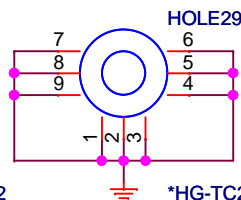
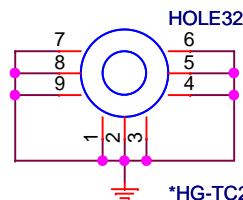
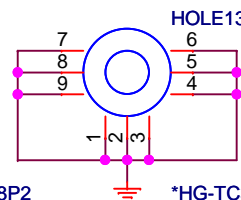
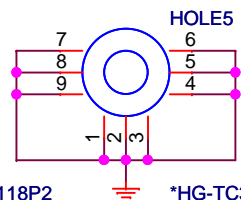
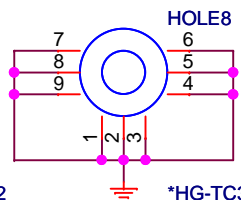
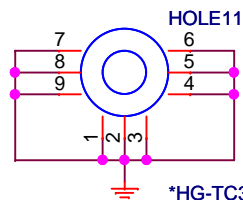
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